

# Discrete/UMA Schematics Document

## Sandy Bridge

### Intel PCH

### 2011-01-04

### REV : A00

*DY :None Installed*

*UMA:UMA ONLY installed*

*DN15: ONLY FOR DN15 installed.*

*DQ15:ONLY FOR DQ15 installed.*

*PSL: KBC795 PSL circuit for 10mW solution installed.*

*10mW: External circuit for 10mW solution installed.*

*MUXLESS:MUXLESS solution installed.*

*OPTIMUS:OPTIMUS solution installed.*

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size

A3

Document Number

**QUEEN 15**

Rev

**A00**

Date: Tuesday, January 04, 2011

Sheet 1 of 108

## Block Diagram

PCB P/N : 10260-1

**Revision : A00**

**SYSTEM LDO**  
APL5916 48

INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0

**SYSTEM DC/DC**  
TPS51218 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

**SYSTEM DC/DC**  
TPS51123RGER 41

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

**SYSTEM DC/DC**  
TPS51216RUKR 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

**SYSTEM DC/DC**  
ISL95831HRTZ 44

INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE

**VGA**  
RT8208B 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

**TI CHARGER**  
BQ24745 40

INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

**SYSTEM DC/DC**  
TPS51311 47

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

**SYSTEM DC/DC**  
G9731 93

INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

**Switches**

INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

**PCB LAYER**

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

**Mini-Card**  
02.11a/b/g

**0/100/1000 NIC**  
Realtek 8111E/8105E

**RJ45 CONN**

**0 FA**

**Mini-Card**  
WWAN

**USB3.0 X2 CONN**

**SIM**

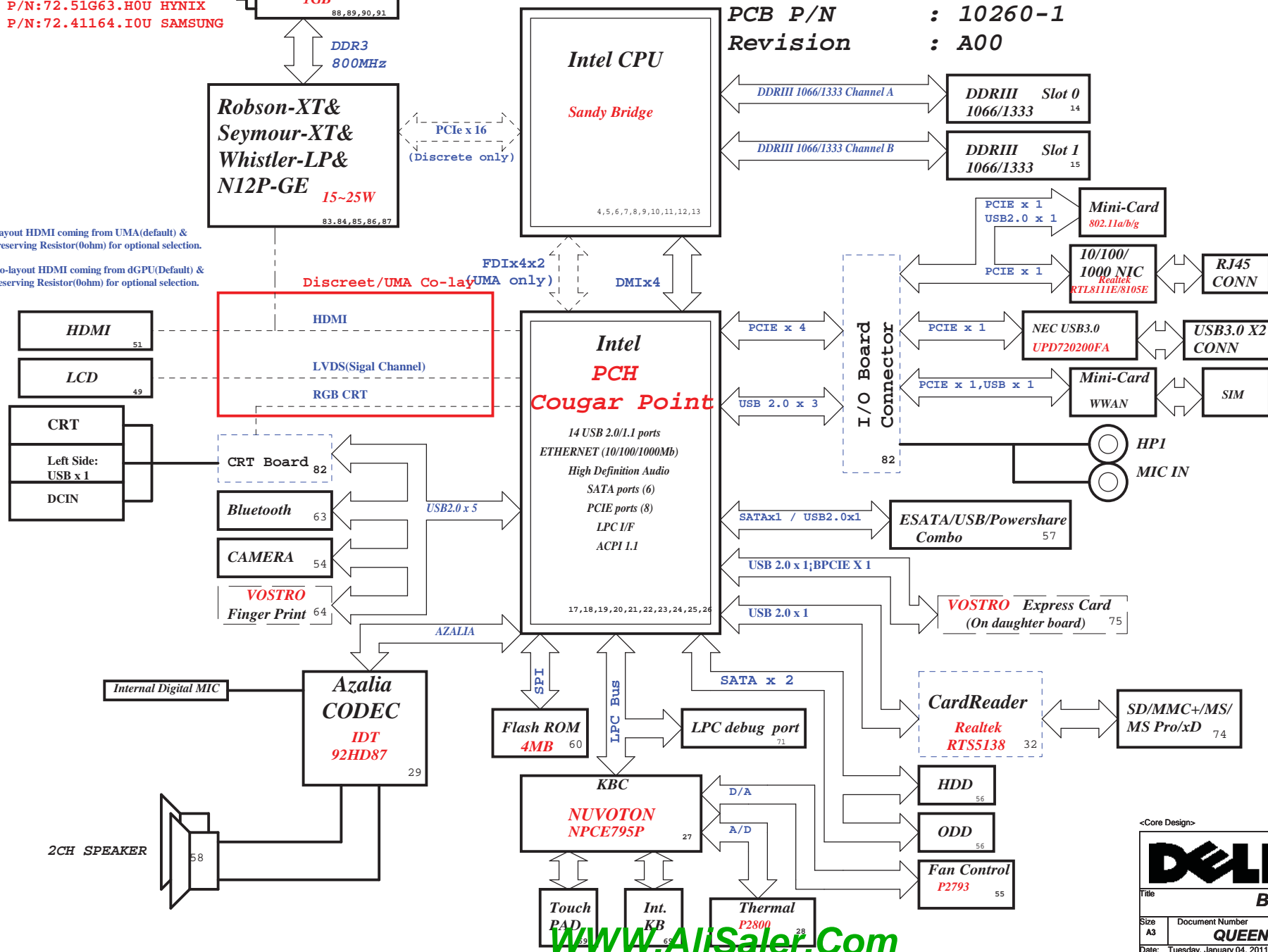
**HP1**

**MIC IN**

**ard**  
75

**SD/MMC+/MS/MS Pro/xD** 74

<Core Design>



A

B

PCH Strapping

Huron River Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kf[ - 10-kf[ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. <b>Disable Danbury:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## USB Table

## PCIE Routing

LANE1	Card Reader
LANE2	Mini Card1(WLAN)
LANE3	Mini Card2(WWAN)
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	Express Card

## SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Car


Processor Strapping				Huron River Schematic Checklist Rev.0_7			
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)		Default Value			
CFG[2]	PCI-Express Static Lane Reversal	1:	Normal Operation.	0:	Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1	
CFG[4]		1:	Disabled - No Physical Display Port attached to Embedded DisplayPort.	0:	Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0	
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 :	x16 - Device 1 functions 1 and 2 disabled	10 :	x8, x8 - Device 1 function 1 enabled ; function 2 disabled	11	
CFG[7]	PEG DEFER TRAINING	01 :	Reserved - (Device 1 function 1 disabled ; function 2 enabled)	00 :	x8, x4, x4 - Device 1 functions 1 and 2 enabled		
		1:	PEG Train immediately following xxRESETB de assertion	0:	PEG Wait for BIOS for training		

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OPAKCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

## SMBus ADDRESSES

I <sup>2</sup> C / SMBus Addresses		Ref Des	HURON RIVER ORB		
Device			Address	Hex	Bus
EC SMBus 1 Battery CHARGER					BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP					SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI					PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		<b>Table of Content</b>	
Size A3	Document Number	Rev	
Date: tuesday, January 04, 2011		Sheet 3	of 108

SSID = CPU

WWW.AliSaler.Com

Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Lane reversal does not apply to FDI sideband signals.

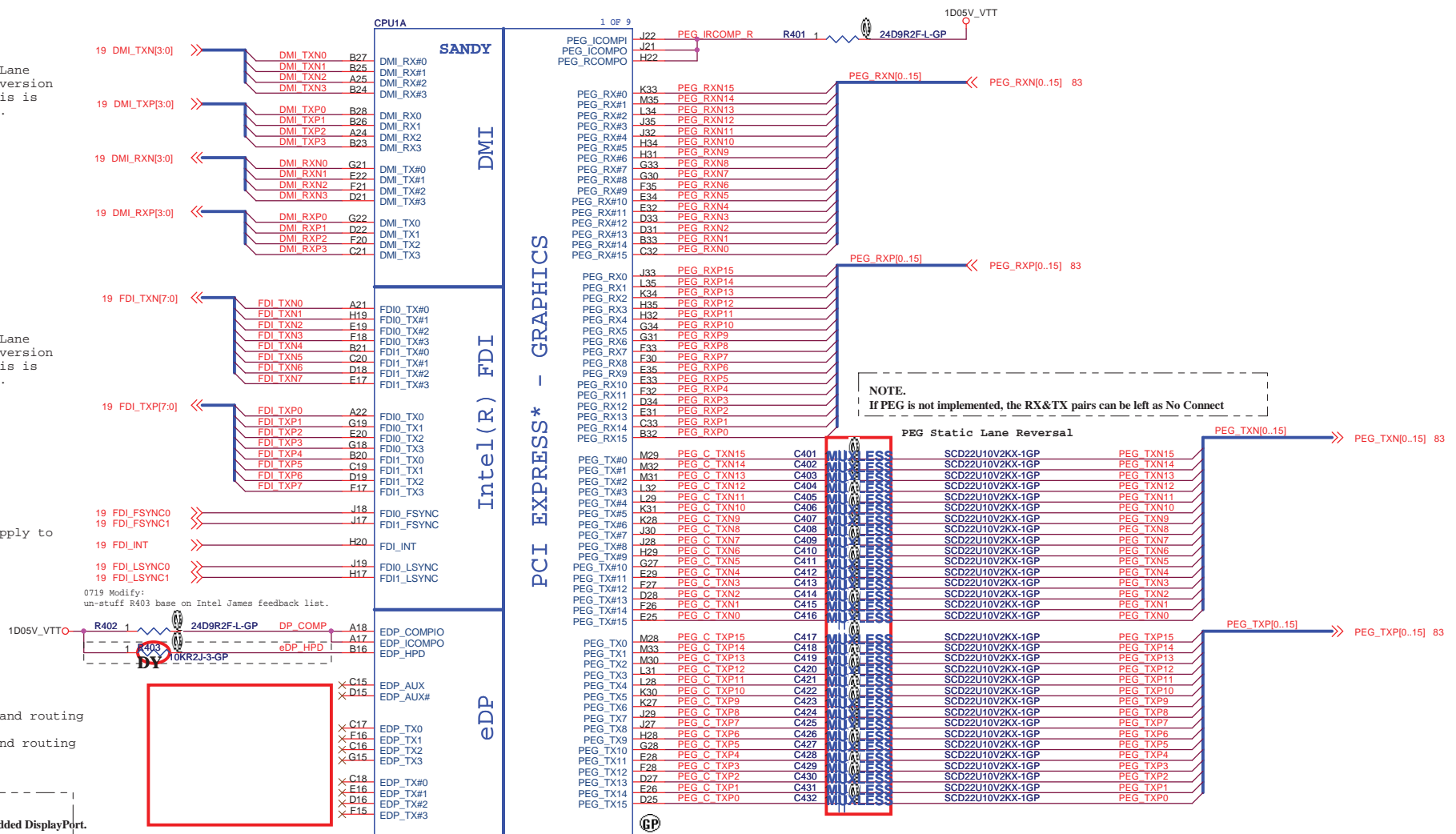
Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

NOTE:  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k $\Omega$  pull-Up resistor on the motherboard.

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



SANDY SKT-BGA989C470395-1H180  
62.10055.421  
2nd = 62.10040.771  
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild hatch run

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**CPU (PCIe/DMI/FDI)**

QUEEN 15

Document Number  
Date: tuesday, January 04, 2011

Rev  
A00

Sheet 4 of 108

WWW.AliSaler.Com

SSID = CPU

WWW.AliSaler.Com

0625 Modify:  
Add C502 47p 0402 on H\_PROCHOT#.

D

C

C

B

A

CPU1B

SANDY

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

BCLK# A28  
BCLK# A27  
DPLL\_REF\_SSCLK A16  
DPLL\_REF\_SSCLK A15

SM\_DRAMRST# R8  
SM\_RCOMP0 A5  
SM\_RCOMP1 A4  
SM\_RCOMP2 A4

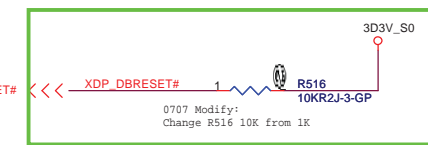
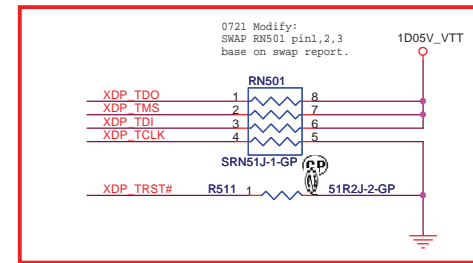
PRDY# AP29  
PREQ# AP27  
TCK AR26  
TMS AR27  
TRST# AP30  
TDI AR28  
TDO AP26

DBR# AL35  
BPM#0 AT28  
BPM#1 AR29  
BPM#2 AR30  
BPM#3 AT30  
BPM#4 AP32  
BPM#5 AR31  
BPM#6 AT31  
BPM#7 AR32

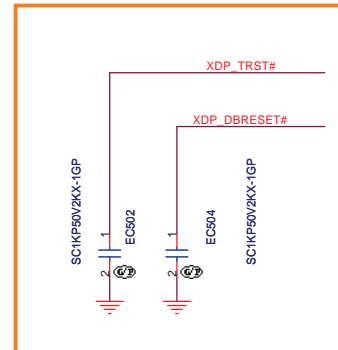
Disabling Guidelines:  
If motherboard only supports external graphics:  
Connect DPLL\_REF\_SSCLK on Processor to GND through  
1K +/- 5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP  
through 1K +/- 5% resistor power (~15 mW) may be  
wasted.

0617 Modify:  
Joseph change RN501 to R512,R514 1K 0402 Resistor.

Signal Routing Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



0630 Modify:  
Removed XDP1101 connector  
related circuit by layout limitation.



A00 1229 EMI

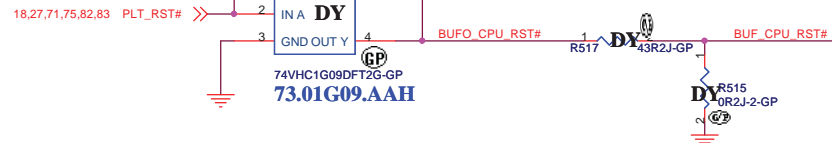
SANDY SKT-BGA989C470395-1H180  
62.10055.421  
2nd = 62.10040.771  
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

0617 Modify:  
Joseph Removed U501 Buffer reset to CPU circuit.

0719 Modify:  
Add buffer for PLT\_RST# based on Intel review.

Buffered reset to CPU

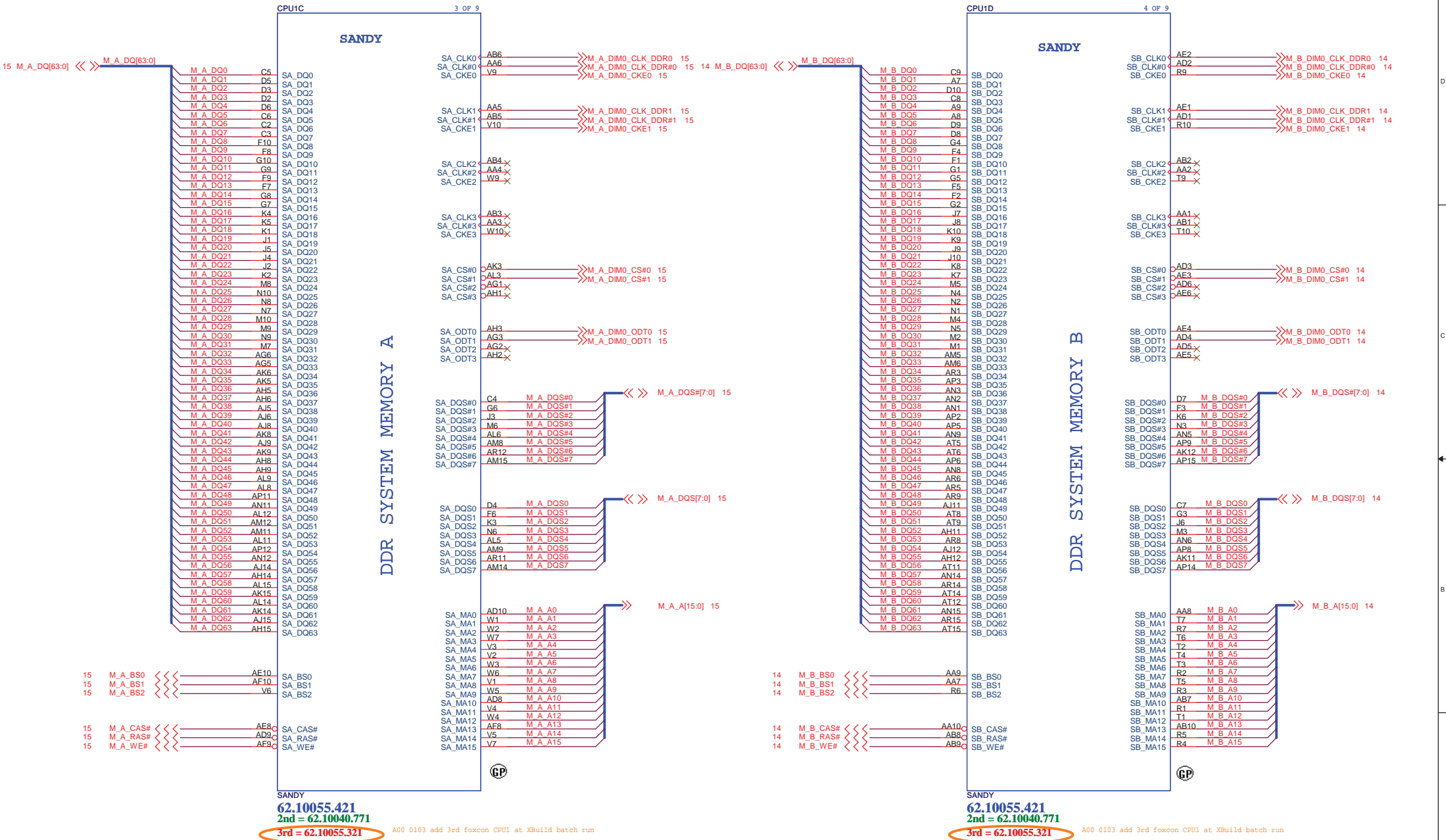


WWW.AliSaler.Com

<Variant Name>

<b>DELL</b> Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CPU (THERMAL/CLOCK/PM)</b>	
Size A3	Document Number <b>QUEEN 15</b>
Date: tuesday, January 04, 2011	Rev <b>A00</b>
Sheet 5 of 108	





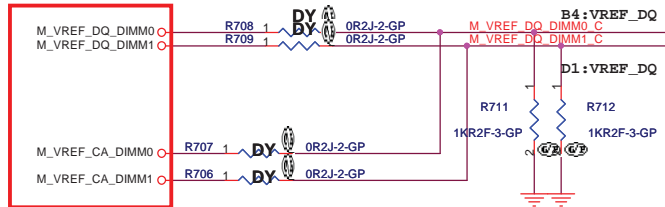
0630 Modify:  
Reserved TP715 on CFG0.

TPAD14-GP TP715

0707 Modify:  
Removed CFG1,CFG3,CFG8-17 TP.

0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0,M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0,M\_VREF\_CA\_DIMM1  
from net to power.

### M3 - Processor Generated SO-DIMM VREF\_DQ



0629 Modify:  
Reserved R710 0ohm to GND to  
follow EV board schematic.



1D05V\_VTT



0719 Modify:  
Reserved EC701 0.1uF near  
R711(BOTTOM) for EMC NEO suggestion.

CPU1E

5 OF 9

SANDY

RESERVED

CFG0  
CFG1  
CFG2  
CFG3  
CFG4  
CFG5  
CFG6  
CFG7  
CFG8  
CFG9  
CFG10  
CFG11  
CFG12  
CFG13  
CFG14  
CFG15  
CFG16  
CFG17

RSVD#AJ31  
RSVD#AH31  
RSVD#AJ33  
RSVD#AH33

RSVD#AJ26

RSVD#B4

RSVD#D1

RSVD#F25

RSVD#F24

RSVD#F23

RSVD#D24

RSVD#G25

RSVD#G24

RSVD#E23

RSVD#D23

RSVD#C30

RSVD#A31

RSVD#B30

RSVD#B29

RSVD#D30

RSVD#B31

RSVD#A30

RSVD#C29

RSVD#J20

RSVD#B18

RSVD#A19

RSVD#J15

RSVD#L7  
RSVD#AG7  
RSVD#AE7  
RSVD#AK2  
RSVD#W8

RSVD#AT26  
RSVD#AM33  
RSVD#AJ27

RSVD#T8  
RSVD#J16  
RSVD#H16  
RSVD#G16

RSVD#AR35  
RSVD#AT34  
RSVD#AT33  
RSVD#AP35  
RSVD#AR34

RSVD#B34  
RSVD#A33  
RSVD#A34  
RSVD#B35  
RSVD#C35

RSVD#AJ32  
RSVD#AK32

RSVD#AH27

RSVD#AN35  
RSVD#AM35

RSVD#AT2  
RSVD#AT1  
RSVD#AR1

GP

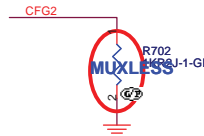
SANDY SGT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

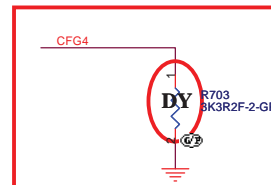
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run



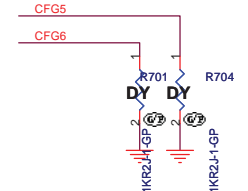
#### PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



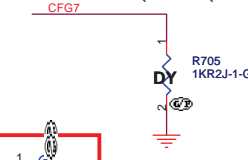
#### Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



#### PCIe Port Bifurcation Straps

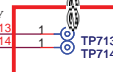
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



#### PEG DEFER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

0702 Modify:  
Reserved TP713  
Reserved TP714



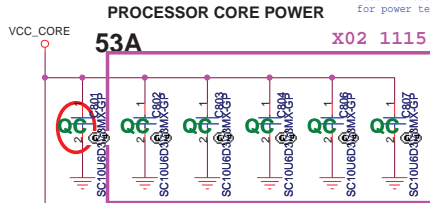
0630 Modify:  
Removed CLK\_XDP\_ITP\_P6N  
and reserved TP713,TP714.

<Variant Name>

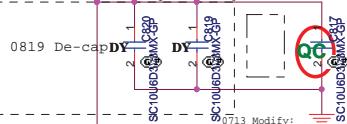
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>CPU (RESERVED)</b>			
Size A3	Document Number	Rev <b>A00</b>	
Date: Tuesday, January 04, 2011		Sheet 7	of 108


Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

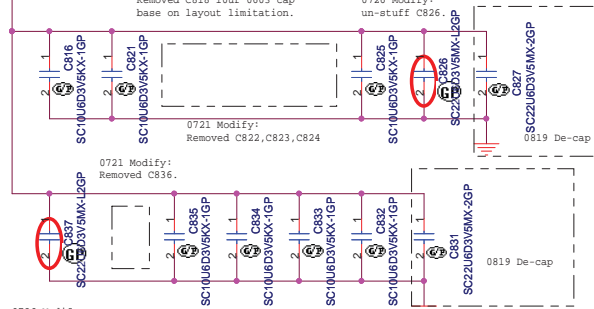
```
1115 X02 Modify:
Reserved C802~C804,C806,C807 10uF 0603
for power team fine tune Vcore quality.
```



0713 Modify:  
Removed C802,C811 10uf 0603  
cap base on layout limitation.



0713 Modify:   
Removed C818 10uf 0603 cap  
base on layout limitation.



```
0726 Modify:
un-stuff C837.
```

VCC Output Decoupling Recommendation:  
4 x 470 uF at Bottom Socket Edge  
8 x 22 uF at Top Socket Cavity  
8 x 22 uF at Top Socket Edge  
8 x 22 uF at Bottom Socket Cavity

VCC\_CORE

## POWER

**SANDY**

## PEG AND DDR

## CORE SUPPLY

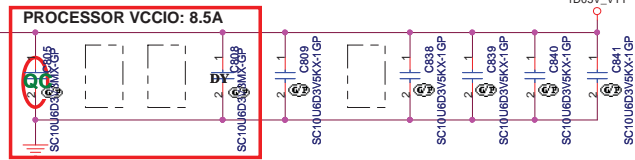
*SVID*

## SENSE LINES

SANDY

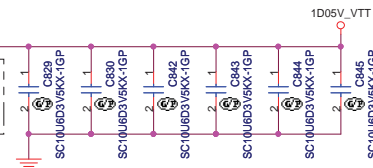
62 1005.42  
2m = 2.1005.72  
card = 2.1005.320  
0 build 3m foxconn China build batch run

VCCIO Output Decoupling Recommendation:  
 2 x 330 uF (3 x 330 uF for 2012 capable designs)  
 5 x 22 uF & 5 x 0805 no-stuff at Bottom  
 7 x 22 uF & 2 x 0805 no-stuff at Top

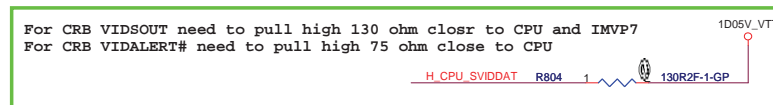


0713 Modify:  
Removed C810,C806,C807 10uf 0603 cap  
base on layout limitation.

No-stuff sites outside the socket may be removed.  
No-stuff sites inside the socket cavity need to remain.

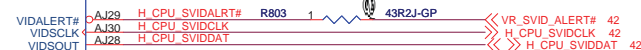


17 Modify:  
 Graph Removed C812  
 13,C814

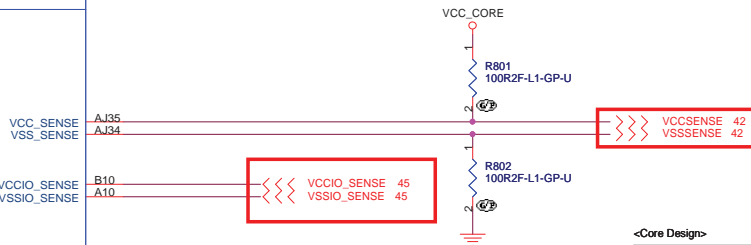


20100610 V1.0

0705 Modify:  
Removed R805,R806, already PH closed PWM side.



VIDALERT#	AJ29	H. CPU SVIDALRT#	R803	1		43R2J-GP	VR_SVID_ALERT#	42
VIDSCLK	AJ30	H. CPU SVIDCLK					H. CPU SVIDCLK	42
VIDSOUT	AJ28	H. CPU SVIDDAT					H. CPU SVIDDAT	42



&amp;ltCore Design&gt;

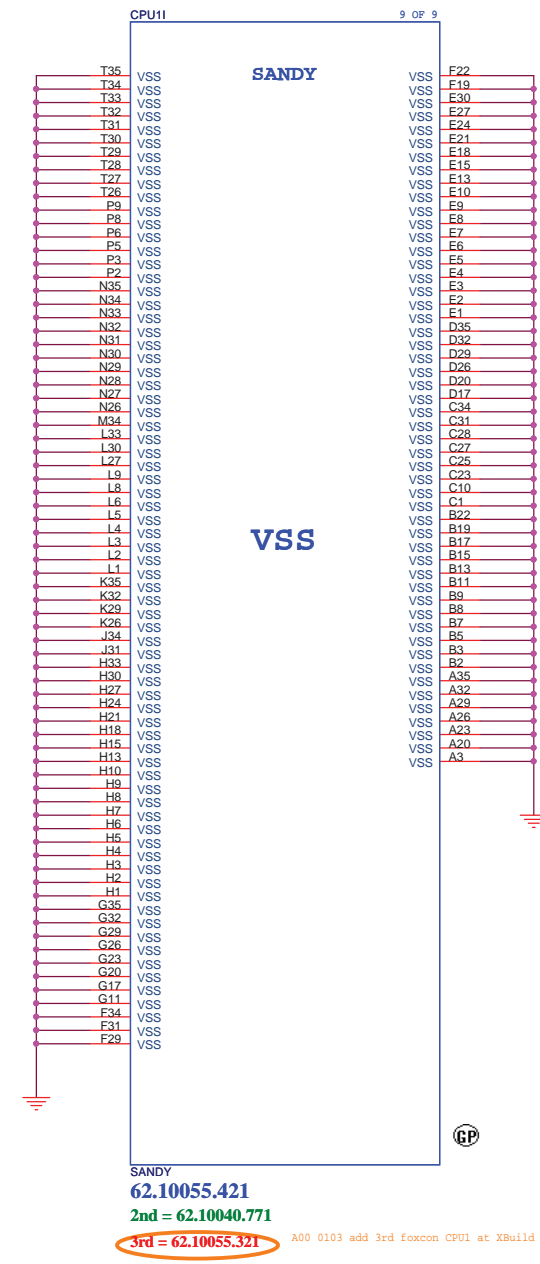
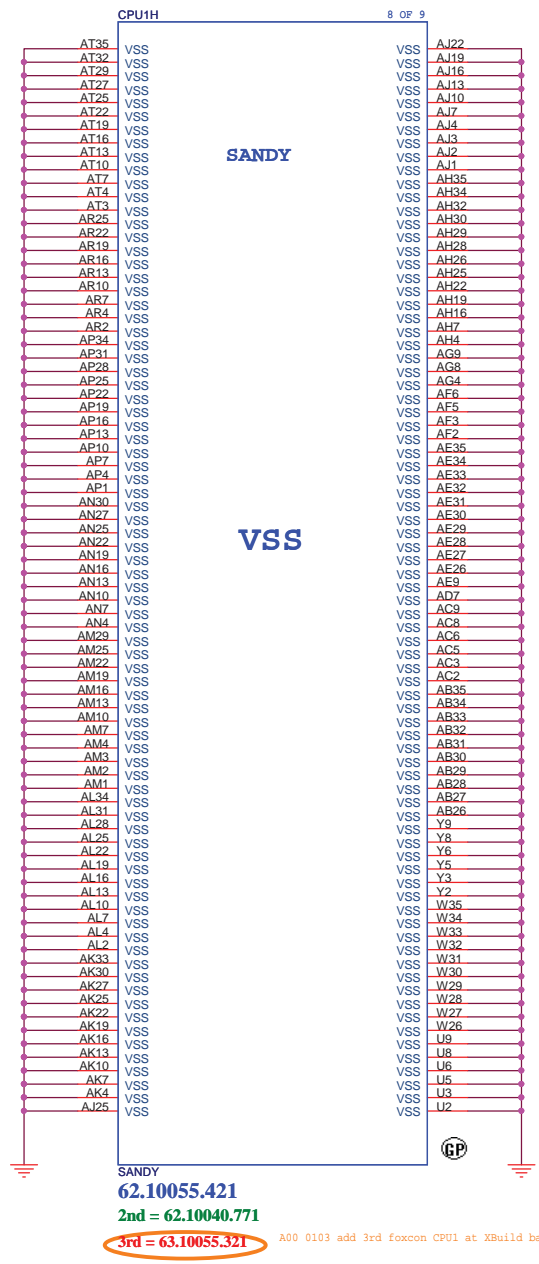


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>CPU (VCC CORE)</b>			
Size	Document Number		Rev
Custom	<b>QUEEN 15</b>		<b>A00</b>
Date:	Tuesday, January 04, 2011	Sheet 8 of	108







<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size A3

Document Number

QUEEN 15


Date: Tuesday, January 04, 2011

Sheet 10 of 108

Rev A00

(Blanking)

<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

***XDP***

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 11 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 12 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

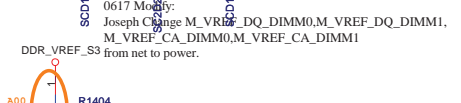
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 13 of	108

0624 Modify:  
SWAP DM1 and DM2 location.

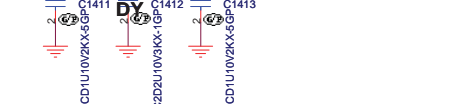
0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



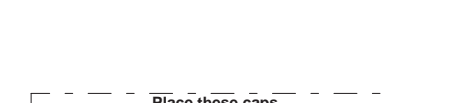
0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



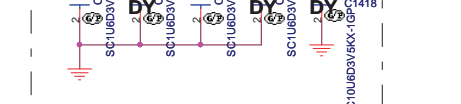
0707 Modify:  
Change R1404, R1405 to 0ohm 0402 from short pad.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



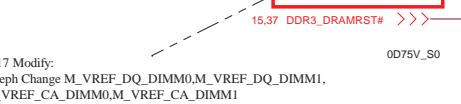
0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.

- M\_B A0 98
- M\_B A1 97
- M\_B A2 96
- M\_B A3 95
- M\_B A4 94
- M\_B A5 93
- M\_B A6 92
- M\_B A7 91
- M\_B A8 90
- M\_B A9 89
- M\_B A10 88
- M\_B A11 87
- M\_B A12 86
- M\_B A13 85
- M\_B A14 84
- M\_B A15 83
- M\_B A16 82
- M\_B A17 81
- M\_B A18 80
- M\_B A19 79
- M\_B A20 78
- M\_B A21 77
- M\_B A22 76
- M\_B A23 75
- M\_B A24 74
- M\_B A25 73
- M\_B A26 72
- M\_B A27 71
- M\_B A28 70
- M\_B A29 69
- M\_B A30 68
- M\_B A31 67
- M\_B A32 66
- M\_B A33 65
- M\_B A34 64
- M\_B A35 63
- M\_B A36 62
- M\_B A37 61
- M\_B A38 60
- M\_B A39 59
- M\_B A40 58
- M\_B A41 57
- M\_B A42 56
- M\_B A43 55
- M\_B A44 54
- M\_B A45 53
- M\_B A46 52
- M\_B A47 51
- M\_B A48 50
- M\_B A49 49
- M\_B A50 48
- M\_B A51 47
- M\_B A52 46
- M\_B A53 45
- M\_B A54 44
- M\_B A55 43
- M\_B A56 42
- M\_B A57 41
- M\_B A58 40
- M\_B A59 39
- M\_B A60 38
- M\_B A61 37
- M\_B A62 36
- M\_B A63 35
- M\_B A64 34
- M\_B A65 33
- M\_B A66 32
- M\_B A67 31
- M\_B A68 30
- M\_B A69 29
- M\_B A70 28
- M\_B A71 27
- M\_B A72 26
- M\_B A73 25
- M\_B A74 24
- M\_B A75 23
- M\_B A76 22
- M\_B A77 21
- M\_B A78 20
- M\_B A79 19
- M\_B A80 18
- M\_B A81 17
- M\_B A82 16
- M\_B A83 15
- M\_B A84 14
- M\_B A85 13
- M\_B A86 12
- M\_B A87 11
- M\_B A88 10
- M\_B A89 9
- M\_B A90 8
- M\_B A91 7
- M\_B A92 6
- M\_B A93 5
- M\_B A94 4
- M\_B A95 3
- M\_B A96 2
- M\_B A97 1
- M\_B A98 0

- M\_B BS2 6
- M\_B BS1 6
- M\_B DQ[63:0] 6

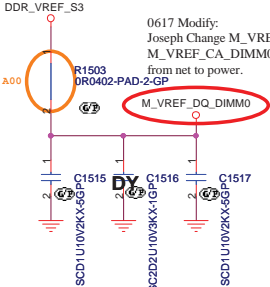
- M\_B DQ0 109
- M\_B DQ1 108
- M\_B DQ2 107
- M\_B DQ3 106
- M\_B DQ4 105
- M\_B DQ5 104
- M\_B DQ6 103
- M\_B DQ7 102
- M\_B DQ8 101
- M\_B DQ9 100
- M\_B DQ10 99
- M\_B DQ11 98
- M\_B DQ12 97
- M\_B DQ13 96
- M\_B DQ14 95
- M\_B DQ15 94
- M\_B DQ16 93
- M\_B DQ17 92
- M\_B DQ18 91
- M\_B DQ19 90
- M\_B DQ20 89
- M\_B DQ21 88
- M\_B DQ22 87
- M\_B DQ23 86
- M\_B DQ24 85
- M\_B DQ25 84
- M\_B DQ26 83
- M\_B DQ27 82
- M\_B DQ28 81
- M\_B DQ29 80
- M\_B DQ30 79
- M\_B DQ31 78
- M\_B DQ32 77
- M\_B DQ33 76
- M\_B DQ34 75
- M\_B DQ35 74
- M\_B DQ36 73
- M\_B DQ37 72
- M\_B DQ38 71
- M\_B DQ39 70
- M\_B DQ40 69
- M\_B DQ41 68
- M\_B DQ42 67
- M\_B DQ43 66
- M\_B DQ44 65
- M\_B DQ45 64
- M\_B DQ46 63
- M\_B DQ47 62
- M\_B DQ48 61
- M\_B DQ49 60
- M\_B DQ50 59
- M\_B DQ51 58
- M\_B DQ52 57
- M\_B DQ53 56
- M\_B DQ54 55
- M\_B DQ55 54
- M\_B DQ56 53
- M\_B DQ57 52
- M\_B DQ58 51
- M\_B DQ59 50
- M\_B DQ60 49
- M\_B DQ61 48
- M\_B DQ62 47
- M\_B DQ63 46
- M\_B DQ64 45
- M\_B DQ65 44
- M\_B DQ66 43
- M\_B DQ67 42
- M\_B DQ68 41
- M\_B DQ69 40
- M\_B DQ70 39
- M\_B DQ71 38
- M\_B DQ72 37
- M\_B DQ73 36
- M\_B DQ74 35
- M\_B DQ75 34
- M\_B DQ76 33
- M\_B DQ77 32
- M\_B DQ78 31
- M\_B DQ79 30
- M\_B DQ80 29
- M\_B DQ81 28
- M\_B DQ82 27
- M\_B DQ83 26
- M\_B DQ84 25
- M\_B DQ85 24
- M\_B DQ86 23
- M\_B DQ87 22
- M\_B DQ88 21
- M\_B DQ89 20
- M\_B DQ90 19
- M\_B DQ91 18
- M\_B DQ92 17
- M\_B DQ93 16
- M\_B DQ94 15
- M\_B DQ95 14
- M\_B DQ96 13
- M\_B DQ97 12
- M\_B DQ98 11
- M\_B DQ99 10
- M\_B DQ100 9
- M\_B DQ101 8
- M\_B DQ102 7
- M\_B DQ103 6
- M\_B DQ104 5
- M\_B DQ105 4
- M\_B DQ106 3
- M\_B DQ107 2
- M\_B DQ108 1
- M\_B DQ109 0

- M\_B DQS#0 10
- M\_B DQS#1 27
- M\_B DQS#2 45
- M\_B DQS#3 62
- M\_B DQS#4 135
- M\_B DQS#5 152
- M\_B DQS#6 169
- M\_B DQS#7 186
- M\_B DQS#8 10
- M\_B DQS#9 27
- M\_B DQS#10 45
- M\_B DQS#11 62
- M\_B DQS#12 135
- M\_B DQS#13 152
- M\_B DQS#14 169
- M\_B DQS#15 186
- M\_B DQS#16 10
- M\_B DQS#17 27
- M\_B DQS#18 45
- M\_B DQS#19 62
- M\_B DQS#20 135
- M\_B DQS#21 152
- M\_B DQS#22 169
- M\_B DQS#23 186
- M\_B DQS#24 10
- M\_B DQS#25 27
- M\_B DQS#26 45
- M\_B DQS#27 62
- M\_B DQS#28 135
- M\_B DQS#29 152
- M\_B DQS#30 169
- M\_B DQS#31 186
- M\_B DQS#32 10
- M\_B DQS#33 27
- M\_B DQS#34 45
- M\_B DQS#35 62
- M\_B DQS#36 135
- M\_B DQS#37 152
- M\_B DQS#38 169
- M\_B DQS#39 186
- M\_B DQS#40 10
- M\_B DQS#41 27
- M\_B DQS#42 45
- M\_B DQS#43 62
- M\_B DQS#44 135
- M\_B DQS#45 152
- M\_B DQS#46 169
- M\_B DQS#47 186
- M\_B DQS#48 10
- M\_B DQS#49 27
- M\_B DQS#50 45
- M\_B DQS#51 62
- M\_B DQS#52 135
- M\_B DQS#53 152
- M\_B DQS#54 169
- M\_B DQS#55 186
- M\_B DQS#56 10
- M\_B DQS#57 27
- M\_B DQS#58 45
- M\_B DQS#59 62
- M\_B DQS#60 135
- M\_B DQS#61 152
- M\_B DQS#62 169
- M\_B DQS#63 186
- M\_B DQS#64 10
- M\_B DQS#65 27
- M\_B DQS#66 45
- M\_B DQS#67 62
- M\_B DQS#68 135
- M\_B DQS#69 152
- M\_B DQS#70 169
- M\_B DQS#71 186
- M\_B DQS#72 10
- M\_B DQS#73 27
- M\_B DQS#74 45
- M\_B DQS#75 62
- M\_B DQS#76 135
- M\_B DQS#77 152
- M\_B DQS#78 169
- M\_B DQS#79 186
- M\_B DQS#80 10
- M\_B DQS#81 27
- M\_B DQS#82 45
- M\_B DQS#83 62
- M\_B DQS#84 135
- M\_B DQS#85 152
- M\_B DQS#86 169
- M\_B DQS#87 186
- M\_B DQS#88 10
- M\_B DQS#89 27
- M\_B DQS#90 45
- M\_B DQS#91 62
- M\_B DQS#92 135
- M\_B DQS#93 152
- M\_B DQS#94 169
- M\_B DQS#95 186
- M\_B DQS#96 10
- M\_B DQS#97 27
- M\_B DQS#98 45
- M\_B DQS#99 62
- M\_B DQS#100 135
- M\_B DQS#101 152
- M\_B DQS#102 169
- M\_B DQS#103 186
- M\_B DQS#104 10
- M\_B DQS#105 27
- M\_B DQS#106 45
- M\_B DQS#107 62
- M\_B DQS#108 135
- M\_B DQS#109 152
- M\_B DQS#110 169
- M\_B DQS#111 186
- M\_B DQS#112 10
- M\_B DQS#113 27
- M\_B DQS#114 45
- M\_B DQS#115 62
- M\_B DQS#116 135
- M\_B DQS#117 152
- M\_B DQS#118 169
- M\_B DQS#119 186
- M\_B DQS#120 10
- M\_B DQS#121 27
- M\_B DQS#122 45
- M\_B DQS#123 62
- M\_B DQS#124 135
- M\_B DQS#125 152
- M\_B DQS#126 169
- M\_B DQS#127 186
- M\_B DQS#128 10
- M\_B DQS#129 27
- M\_B DQS#130 45
- M\_B DQS#131 62
- M\_B DQS#132 135
- M\_B DQS#133 152
- M\_B DQS#134 169
- M\_B DQS#135 186
- M\_B DQS#136 10
- M\_B DQS#137 27
- M\_B DQS#138 45
- M\_B DQS#139 62
- M\_B DQS#140 135
- M\_B DQS#141 152
- M\_B DQS#142 169
- M\_B DQS#143 186
- M\_B DQS#144 10
- M\_B DQS#145 27
- M\_B DQS#146 45
- M\_B DQS#147 62
- M\_B DQS#148 135
- M\_B DQS#149 152
- M\_B DQS#150 169
- M\_B DQS#151 186
- M\_B DQS#152 10
- M\_B DQS#153 27
- M\_B DQS#154 45
- M\_B DQS#155 62
- M\_B DQS#156 135
- M\_B DQS#157 152
- M\_B DQS#158 169
- M\_B DQS#159 186
- M\_B DQS#160 10
- M\_B DQS#161 27
- M\_B DQS#162 45
- M\_B DQS#163 62
- M\_B DQS#164 135
- M\_B DQS#165 152
- M\_B DQS#166 169
- M\_B DQS#167 186
- M\_B DQS#168 10
- M\_B DQS#169 27
- M\_B DQS#170 45
- M\_B DQS#171 62
- M\_B DQS#172 135
- M\_B DQS#173 152
- M\_B DQS#174 169
- M\_B DQS#175 186
- M\_B DQS#176 10
- M\_B DQS#177 27
- M\_B DQS#178 45
- M\_B DQS#179 62
- M\_B DQS#180 135
- M\_B DQS#181 152
- M\_B DQS#182 169
- M\_B DQS#183 186
- M\_B DQS#184 10
- M\_B DQS#185 27
- M\_B DQS#186 45
- M\_B DQS#187 62
- M\_B DQS#188 135
- M\_B DQS#189 152
- M\_B DQS#190 169
- M\_B DQS#191 186
- M\_B DQS#192 10
- M\_B DQS#193 27
- M\_B DQS#194 45
- M\_B DQS#195 62
- M\_B DQS#196 135
- M\_B DQS#197 152
- M\_B DQS#198 169
- M\_B DQS#199 186
- M\_B DQS#200 10
- M\_B DQS#201 27
- M\_B DQS#202 45
- M\_B DQS#203 62
- M\_B DQS#204 135
- M\_B DQS#205 152
- M\_B DQS#206 169
- M\_B DQS#207 186
- M\_B DQS#208 10
- M\_B DQS#209 27
- M\_B DQS#210 45
- M\_B DQS#211 62
- M\_B DQS#212 135
- M\_B DQS#213 152
- M\_B DQS#214 169
- M\_B DQS#215 186
- M\_B DQS#216 10
- M\_B DQS#217 27
- M\_B DQS#218 45
- M\_B DQS#219 62
- M\_B DQS#220 135
- M\_B DQS#221 152
- M\_B DQS#222 169
- M\_B DQS#223 186
- M\_B DQS#224 10
- M\_B DQS#225 27
- M\_B DQS#226 45
- M\_B DQS#227 62
- M\_B DQS#228 135
- M\_B DQS#229 152
- M\_B DQS#230 169
- M\_B DQS#231 186
- M\_B DQS#232 10
- M\_B DQS#233 27
- M\_B DQS#234 45
- M\_B DQS#235 62
- M\_B DQS#236 135
- M\_B DQS#237 152
- M\_B DQS#238 169
- M\_B DQS#239 186
- M\_B DQS#240 10
- M\_B DQS#241 27
- M\_B DQS#242 45
- M\_B DQS#243 62
- M\_B DQS#244 135
- M\_B DQS#245 152
- M\_B DQS#246 169
- M\_B DQS#247 186
- M\_B DQS#248 10
- M\_B DQS#249 27
- M\_B DQS#250 45
- M\_B DQS#251 62
- M\_B DQS#252 135
- M\_B DQS#253 152
- M\_B DQS#254 169
- M\_B DQS#255 186
- M\_B DQS#256 10
- M\_B DQS#257 27
- M\_B DQS#258 45
- M\_B DQS#259 62
- M\_B DQS#260 135
- M\_B DQS#261 152
- M\_B DQS#262 169
- M\_B DQS#263 186
- M\_B DQS#264 10
- M\_B DQS#265 27
- M\_B DQS#266 45
- M\_B DQS#267 62
- M\_B DQS#268 135
- M\_B DQS#269 152
- M\_B DQS#270 169
- M\_B DQS#271 186
- M\_B DQS#272 10
- M\_B DQS#273 27
- M\_B DQS#274 45
- M\_B DQS#275 62
- M\_B DQS#276 135
- M\_B DQS#277 152
- M\_B DQS#278 169
- M\_B DQS#279 186
- M\_B DQS#280 10
- M\_B DQS#281 27
- M\_B DQS#282 45
- M\_B DQS#283 62
- M\_B DQS#284 135
- M\_B DQS#285 152
- M\_B DQS#286 169
- M\_B DQS#287 186
- M\_B DQS#288 10
- M\_B DQS#289 27
- M\_B DQS#290 45
- M\_B DQS#291 62
- M\_B DQS#292 135
- M\_B DQS#293 152
- M\_B DQS#294 169
- M\_B DQS#295 186
- M\_B DQS#296 10
- M\_B DQS#297 27
- M\_B DQS#298 45
- M\_B DQS#299 62
- M\_B DQS#300 135
- M\_B DQS#301 152
- M\_B DQS#302 169
- M\_B DQS#303 186
- M\_B DQS#304 10
- M\_B DQS#305 27
- M\_B DQS#306 45
- M\_B DQS#307 62
- M\_B DQS#308 135
- M\_B DQS#309 152
- M\_B DQS#310 169
- M\_B DQS#311 186
- M\_B DQS#312 10
- M\_B DQS#313 27
- M\_B DQS#314 45
- M\_B DQS#315 62
- M\_B DQS#316 135
- M\_B DQS#317 152
- M\_B DQS#318 169
- M\_B DQS#319 186
- M\_B DQS#320 10
- M\_B DQS#321 27
- M\_B DQS#322 45
- M\_B DQS#323 62
- M\_B DQS#324 135
- M\_B DQS#325 152
- M\_B DQS#326 169
- M\_B DQS#327 186
- M\_B DQS#328 10
- M\_B DQS#329 27
- M\_B DQS#330 45
- M\_B DQS#331 62
- M\_B DQS#332 135
- M\_B DQS#333 152
- M\_B DQS#334 169
- M\_B DQS#335 186
- M\_B DQS#336 10
- M\_B DQS#337 27
- M\_B DQS#338 45
- M\_B DQS#339 62
- M\_B DQS#340 135
- M\_B DQS#341 152
- M\_B DQS#342 169
- M\_B DQS#343 186
- M\_B DQS#344 10
- M\_B DQS#345 27
- M\_B DQS#346 45
- M\_B DQS#347 62
- M\_B DQS#348 135
- M\_B DQS#349 152
- M\_B DQS#350 169
- M\_B DQS#351 186
- M\_B DQS#352 10
- M\_B DQS#353 27
- M\_B DQS#354 45
- M\_B DQS#355 62
- M\_B DQS#356 135
- M\_B DQS#357 152
- M\_B DQS#358 169
- M\_B DQS#359 186
- M\_B DQS#360 10
- M\_B DQS#361 27
- M\_B DQS#362 45
- M\_B DQS#363 62
- M\_B DQS#364 135
- M\_B DQS#365 152
- M\_B DQS#366 169
- M\_B DQS#367 186
- M\_B DQS#368 10
- M\_B DQS#369 27
- M\_B DQS#370 45
- M\_B DQS#371 62
- M\_B DQS#372 135
- M\_B DQS#373 152
- M\_B DQS#374 169
- M\_B DQS#375 186
- M\_B DQS#376 10
- M\_B DQS#377 27
- M\_B DQS#378 45
- M\_B DQS#379 62
- M\_B DQS#380 135
- M\_B DQS#381 152
- M\_B DQS#382 169
- M\_B DQS#383 186
- M\_B DQS#384 10
- M\_B DQS#385 27
- M\_B DQS#386 45
- M\_B DQS#387 62
- M\_B DQS#388 135
- M\_B DQS#389 152
- M\_B DQS#390 169
- M\_B DQS#391 186
- M\_B DQS#392 10
- M\_B DQS#393 27
- M\_B DQS#394 45
- M\_B DQS#395 62
- M\_B DQS#396 135
- M\_B DQS#397 152
- M\_B DQS#398 169
- M\_B DQS#399 186
- M\_B DQS#400 10
- M\_B DQS#401 27
- M\_B DQS#402 45
- M\_B DQS#403 62
- M\_B DQS#404 135
- M\_B DQS#405 152
- M\_B DQS#406 169
- M\_B DQS#407 186
- M\_B DQS#408 10
- M\_B DQS#409 27
- M\_B DQS#410 45
- M\_B DQS#411 62
- M\_B DQS#412 135
- M\_B DQS#413 152
- M\_B DQS#414 169
- M\_B DQS#415 186
- M\_B DQS#416 10
- M\_B DQS#417 27
- M\_B DQS#418 45
- M\_B DQS#419 62
- M\_B DQS#420 135
- M\_B DQS#421 152
- M\_B DQS#422 169
- M\_B DQS#423 186
- M\_B DQS#424 10
- M\_B DQS#425 27
- M\_B DQS#426 45
- M\_B DQS#427 62
- M\_B DQS#428 135
- M\_B DQS#429 152
- M\_B DQS#430 169
- M\_B DQS#431 186
- M\_B DQS#432 10
- M\_B DQS#433 27
- M\_B DQS#434 45
- M\_B DQS#435 62
- M\_B DQS#436 135
- M\_B DQS#437 152
- M\_B DQS#438 169
- M\_B DQS#439 186
- M\_B DQS#440 10
- M\_B DQS#441 27
- M\_B DQS#442 45
- M\_B DQS#443 62
- M\_B DQS#444 135
- M\_B DQS#445 152
- M\_B DQS#446 169
- M\_B DQS#447 186
- M\_B DQS#448 10
- M\_B DQS#449 27
- M\_B DQS#450 45
- M\_B DQS#451 62
- M\_B DQS#452 135
- M\_B DQS#453 152
- M\_B DQS#454 169
- M\_B DQS#455 186
- M\_B DQS#456 10
- M\_B DQS#457 27
- M\_B DQS#458 45
- M\_B DQS#459 62
- M\_B DQS#460 135
- M\_B DQS#461 152
- M\_B DQS#462 169
- M\_B DQS#463 186
- M\_B DQS#464 10
- M\_B DQS#465 27
- M\_B DQS#466 45
- M\_B DQS#467 62
- M\_B DQS#468 135
- M\_B DQS#469 152
- M\_B DQS#470 169
- M\_B DQS#471 186
- M\_B DQS#472 10
- M\_B DQS#473 27
- M\_B DQS#474 45
- M\_B DQS#475 62
- M\_B DQS#476 135
- M\_B DQS#477 152
- M\_B DQS#478 169
- M\_B DQS#479 186
- M\_B DQS#480 10
- M\_B DQS#481 27
- M\_B DQS#482 45
- M\_B DQS#483 62
- M\_B DQS#484 135
- M\_B DQS#485 152
- M\_B DQS#486 169
- M\_B DQS#487 186
- M\_B DQS#488 10
- M\_B DQS#489 27
- M\_B DQS#490 45
- M\_B DQS#491 62
- M\_B DQS#492 135
- M\_B DQS#493 152
- M\_B DQS#494 169
- M\_B DQS#495 186
- M\_B DQS#496 10
- M\_B DQS#497 27
- M\_B DQS#498 45
- M\_B DQS#499 62



```
6      M_A_BS2  >>>
6      M_A_BS0  >>>
6      M_A_BS1  <<<<
6      M_A_DQ[63:0] <<<<
```

0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0,M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0,M\_VREF\_CA\_DIMM1  
from net to power.



M\_VREF\_CA\_DIMM0

M\_VREF\_DQ\_DIMM0

0D75V\_S0

H = 9.2mm

62.10017.041

62.10017.Q41  
2nd = 62.10017.N11  
3rd = 62.10017.Nd1  
4th = 62.10017.D91

WWW.AliSaler.Com

A0

NP1	NP2	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	--

```
1110 X02 Modify:
DM1 1st change to 62.10017.Q41; 2nd change
to 62.10017.N11 on ST stage from ME updated
connector list.
```

SO-DIMMB is placed farther from the Processor than SO-DIMMA

The schematic diagram illustrates the power supply section of the 68000 microprocessor. It features a multi-stage voltage regulation circuit. The input from the transformer (T1) is rectified by BR1. The resulting DC voltage is then filtered and regulated through a series of capacitors (C1503, C1504, C1505, C1506, C1507, C1508, C1509, C1510) and diodes (D1503, D1504, D1505, D1506, D1507, D1508, D1509, D1510). The circuit is divided into two sections by a dashed line. The top section, labeled '0818 De-cap', contains capacitors C1503, C1504, C1505, C1506, C1507, C1508, C1509, and C1510, along with diodes D1503, D1504, D1505, D1506, D1507, D1508, D1509, and D1510. The bottom section, labeled '0813 De-cap', contains capacitors C1511, C1512, C1513, C1514, and C1515, along with diodes D1511, D1512, D1513, D1514, and D1515. The output of the top section is connected to the input of the bottom section. The output of the bottom section is connected to the 68000 microprocessor. The 68000 microprocessor is shown with its pins connected to the output of the power supply section.

**Layout Note:**  
Place these Caps near  
SO-DIMMB.


<Variant Name>

**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>DDR3-SODIMM1</b>			
Size	Document Number		Rev
Custom	<b>QUEEN 15</b>		<b>A00</b>
Date:	Tuesday, January 04, 2011	Sheet 15 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

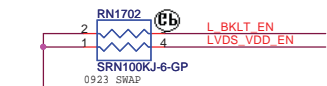
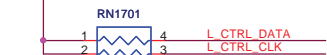
Size  
A3

Document Number  
**QUEEN 15**

Rev  
**A00**

Date: Tuesday, January 04, 2011Sheet 16 of 108

3D3V\_S0

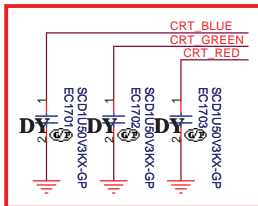
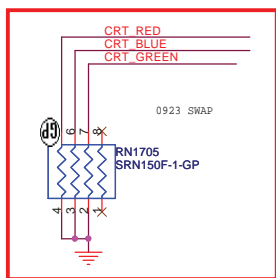


**L\_DDC\_DATA(PAGE17):**  
This signal is on the LVDS interface.  
This signal needs to be left NC if eDP is  
used for the local flat panel display

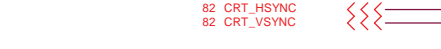
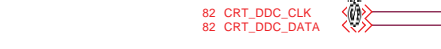
Place near PCH

Impedance: 90 ohm

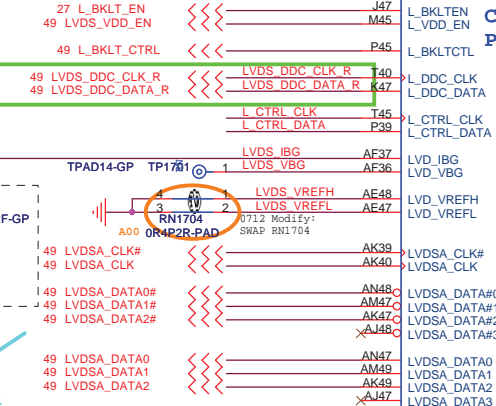
Close to PCH side



0917 X01 Modify:  
Add R1703-R1705 on RGB signal and reserved  
EC1701-EC1703 0.1u from EMC Neo suggestion.



Notes:  
1K 0.5% 0402.  
CHIP RES 1K D 1/16W 0402



Cougar Point

Digital Display Interface

CRT

COUGAR-GP-U2-NF

PCH1D

4 OF 10

L\_BKLTEN  
L\_VDD\_EN

L\_BKLTCTL  
L\_DDC\_CLK  
L\_DDC\_DATA

L\_CTRL\_CLK  
L\_CTRL\_DATA

LVDS\_IBG  
LVDS\_VBG

LVDS\_VREFH  
LVDS\_VREFL

LVDSA\_CLK#  
LVDSA\_CLK

LVDSA\_DATA#0  
LVDSA\_DATA#1  
LVDSA\_DATA#2  
LVDSA\_DATA#3

LVDSA\_DATA0  
LVDSA\_DATA1  
LVDSA\_DATA2  
LVDSA\_DATA3

LVDSB\_CLK#  
LVDSB\_CLK

LVDSB\_DATA#0  
LVDSB\_DATA#1  
LVDSB\_DATA#2  
LVDSB\_DATA#3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

LVDSB\_DATA0  
LVDSB\_DATA1  
LVDSB\_DATA2  
LVDSB\_DATA3

0804 Remove HDMI from PCH.

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_CTRLDATA
	DDPB_HPDP	NA	DDPB_HPDP	HDMI_HPDP
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMI_HPDP

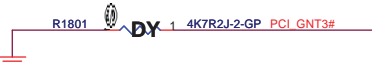
<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

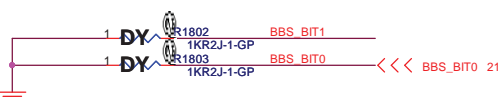
Title	PCH (LVDS/CRT/DDI)		
Size A3	Document Number	QUEEN 15	Rev A00
Date: Tuesday, January 04, 2011	Sheet 17	of 108	

SSID = PCH

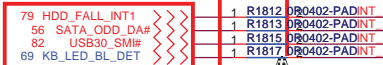
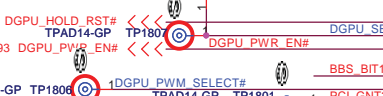
0709 Modify:  
Removed INT\_PIRQ# on RN1801 pin1.



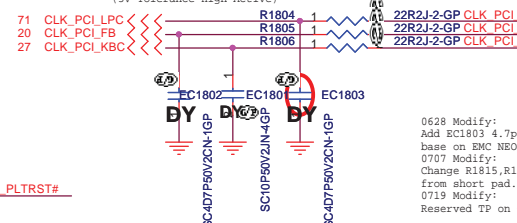
Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



0709 Modify:  
Add R1817 0ohm and connect to KB\_LED\_BL\_DET.  
(5V Tolerance High Active)



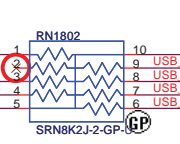
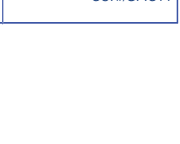
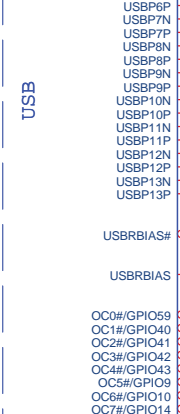
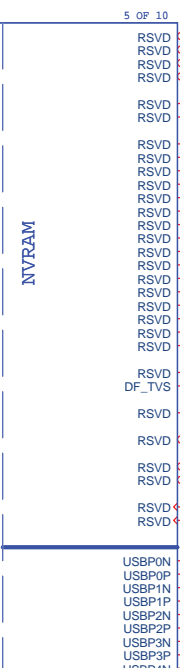
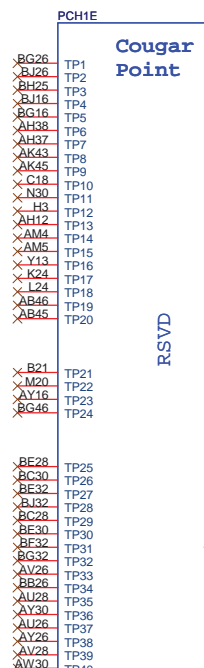
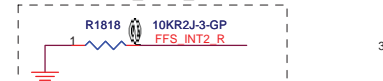
0617 Modify:  
Joseph Remove PLT\_RST AND gate logic IC U1801/C1802.



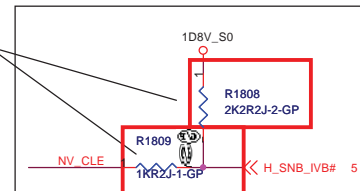
0629 Modify:  
Reserved R1816 100K 0402 on PLT\_RST#



0908 X01 Modify:  
Add R1818 10K PL on FFS\_INT2\_R(GPIO14)



0719 Modify:  
DP\_TVS (NV\_CLR) connect PROC\_SELECT# (H\_SNB\_IVB#) with R1808 2.2K(05% pull up resistor to PCH VCCPAND rail and a R1809 1K(05% series resistor base on Intel feedback.



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB Ext. port 1 (HS)  
External debug port use on Huron river platform

## USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

1120 X02 Modify:  
Reserved USB\_OC#\_1 connect from PCH GPIO59.

## USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

PCH (PCI/USB/NVRAM)			
Size A3	Document Number	Rev	A00
Date: Tuesday, January 04, 2011	QUEEN 15	Sheet 18	of 108

4 DMI\_RXN[3:0] <<< DMI\_RXP[3:0] <<< DMI\_TXN[3:0] <<< DMI\_TXP[3:0] <<<

FDI\_TXN[7:0] 4 FDI\_TXP[7:0] 4

Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI\_RXN0 <<< BC24 DMI0RXN  
4 DMI\_RXN1 <<< BE20 DMI1RXN  
4 DMI\_RXN2 <<< BG18 DMI2RXN  
4 DMI\_RXN3 <<< BG20 DMI3RXN  
4 DMI\_RXP0 <<< BE24 DMI0RXP  
4 DMI\_RXP1 <<< BC20 DMI1RXP  
4 DMI\_RXP2 <<< BJ18 DMI2RXP  
4 DMI\_RXP3 <<< BJ20 DMI3RXP  
4 DMI\_TXN0 <<< AW24 DMI0TXN  
4 DMI\_TXN1 <<< AW20 DMI1TXN  
4 DMI\_TXN2 <<< BB18 DMI2TXN  
4 DMI\_TXN3 <<< AV18 DMI3TXN  
4 DMI\_TXP0 <<< AY24 DMI0TXP  
4 DMI\_TXP1 <<< AY20 DMI1TXP  
4 DMI\_TXP2 <<< AY18 DMI2TXP  
4 DMI\_TXP3 <<< AU18 DMI3TXP

PCH1C

Cougar Point

DMI

FDI

3 OF 10

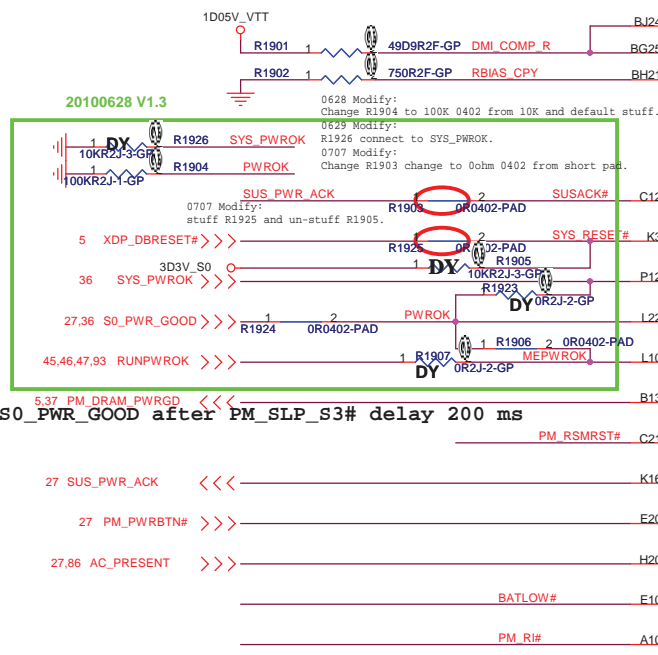
FDI\_RXN0 <<< BJ14 FDI\_TXN0 4  
FDI\_RXN1 <<< AY14 FDI\_TXN1 4  
FDI\_RXN2 <<< BE14 FDI\_TXN2 4  
FDI\_RXN3 <<< BH13 FDI\_TXN3 4  
FDI\_RXN4 <<< BC12 FDI\_TXN4 4  
FDI\_RXN5 <<< BJ12 FDI\_TXN5 4  
FDI\_RXN6 <<< BG10 FDI\_TXN6 4  
FDI\_RXN7 <<< BG9 FDI\_TXN7 4  
FDI\_RXP0 <<< BG14 FDI\_TXP0 4  
FDI\_RXP1 <<< BB14 FDI\_TXP1 4  
FDI\_RXP2 <<< BE14 FDI\_TXP2 4  
FDI\_RXP3 <<< BG13 FDI\_TXP3 4  
FDI\_RXP4 <<< BE12 FDI\_TXP4 4  
FDI\_RXP5 <<< BG12 FDI\_TXP5 4  
FDI\_RXP6 <<< BJ10 FDI\_TXP6 4  
FDI\_RXP7 <<< BH9 FDI\_TXP7 4

FDI\_INT <<< AW16 FDI\_INT 4  
FDI\_FSYNCO <<< AV12 FDI\_FSYNCO 4  
FDI\_FSYNC1 <<< BC10 FDI\_FSYNC1 4  
FDI\_LSYNCO <<< AV14 FDI\_LSYNCO 4  
FDI\_LSYNC1 <<< BB10 FDI\_LSYNC1 4

DSWVRMEN <<< A18 DSWODVREN  
DPWROK <<< E22 PCH\_DPWROK  
WAKE# <<< B9 PCH\_WAKE# 27  
CLKRUN#/GPIO32 <<< N3 PM\_CLKRUN# 27  
SUS\_STAT#/GPIO61 <<< G8 PM\_SUS\_STAT# 1  
SUSCLK#/GPIO62 <<< N14 SUS\_CLK  
SLP\_S5#/GPIO63 <<< D10 PM\_SLP\_S5# 1  
SLP\_S4# <<< H4 PM\_SLP\_S4# 27,46,75  
SLP\_S3# <<< F4 PM\_SLP\_S3# 27,36,37,47,75  
SLP\_A# <<< G10 PM\_SLP\_A# 1  
SLP\_SUS# <<< G16 PM\_SLP\_SUS# 1  
PMSYNCH <<< AP14 H\_PM\_SYNC 5  
SLP\_LAN#/GPIO29 <<< K14 PM\_SLP\_LAN# 1

VccDSW3\_3  
DPWROK  
VccSUS3\_3  
RSMRST#

For platforms not supporting Deep S4/S5  
1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)  
2.DPWROK and RSMRST# will rise at the same time (connected on board)  
3.SLP\_SUS# and SUSACK# are left as ;no connect;,  
4.SUSWARN# used as SUSPWRDNACK/GPIO30

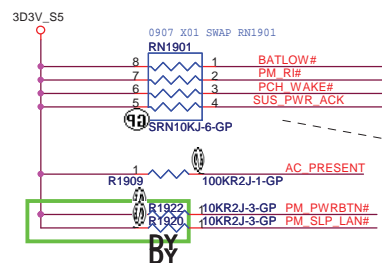


System Power Management

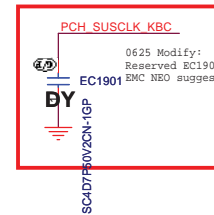
SUSACK#  
SYS\_RESET#  
SYS\_PWROK  
PWROK  
APWROK  
DRAMPWROK  
RSMRST#  
SUSWARN#/SUSPWRDNACK/GPIO30  
PWRBTN#  
ACPRESENT/GPIO31  
BATLOW#/GPIO72  
RI#

COUGAR-GP-U2-NF

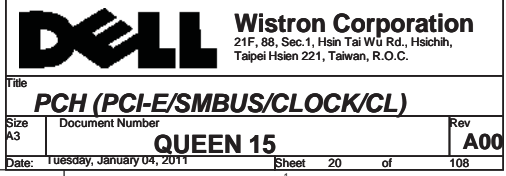
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



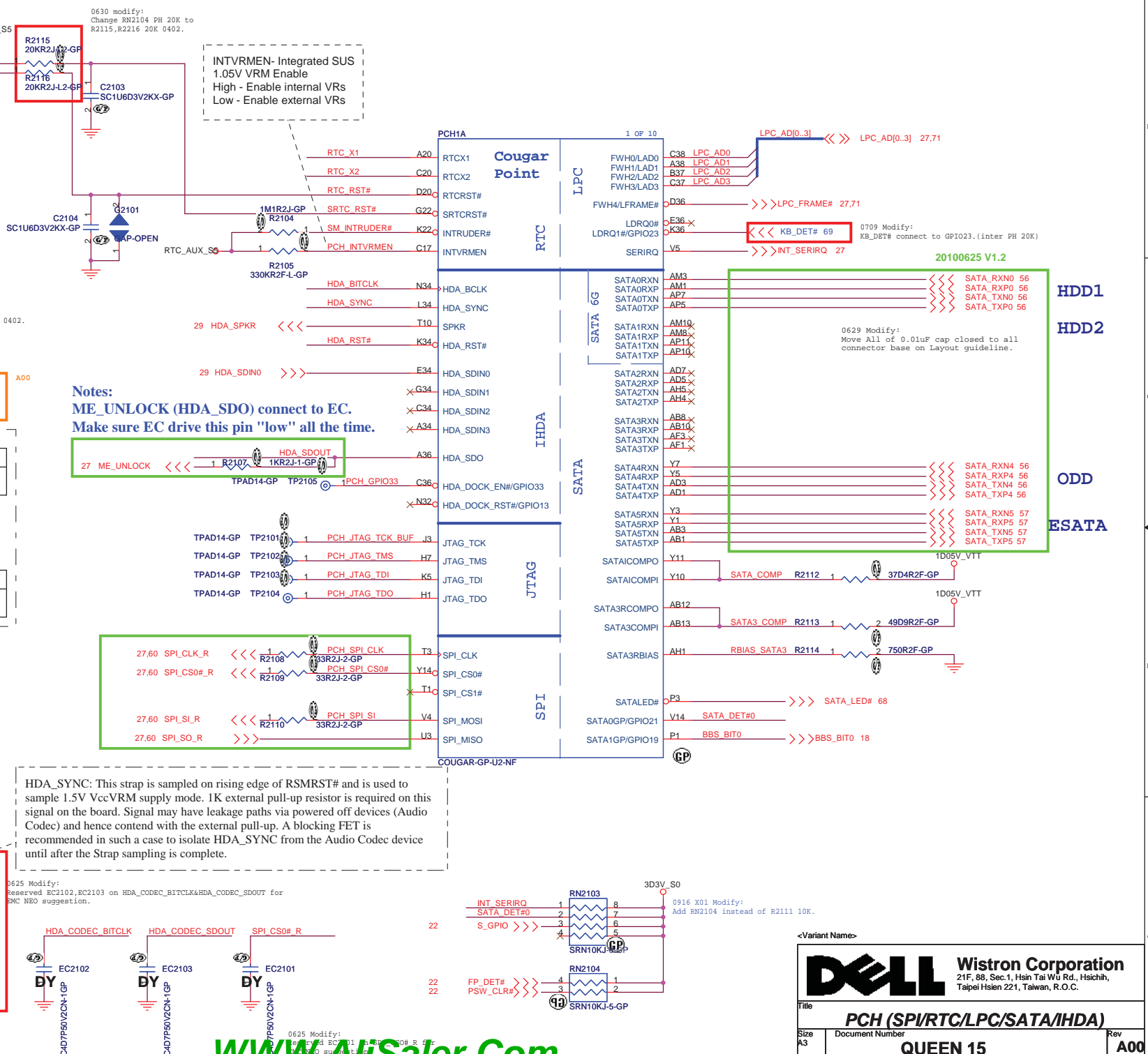
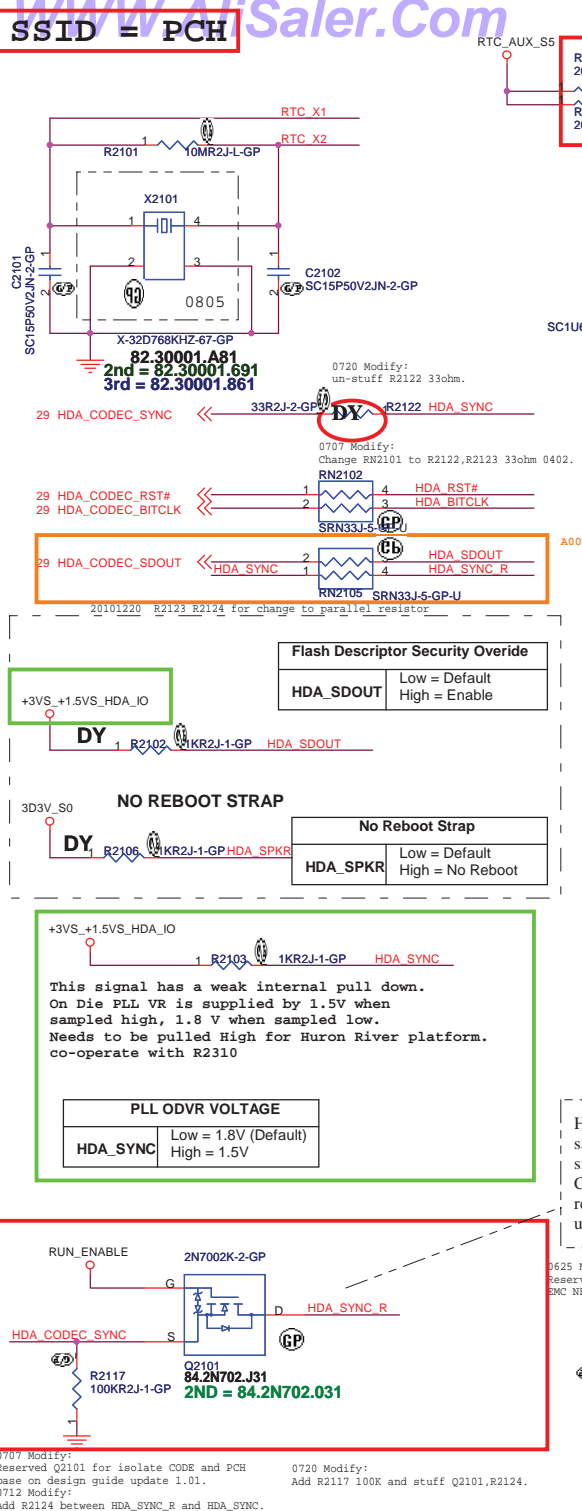
0621 Modify:  
Joseph removed Q1901/R1909/R1916 3V\_5V\_POK  
and PM\_RSMRST# related control circuit.



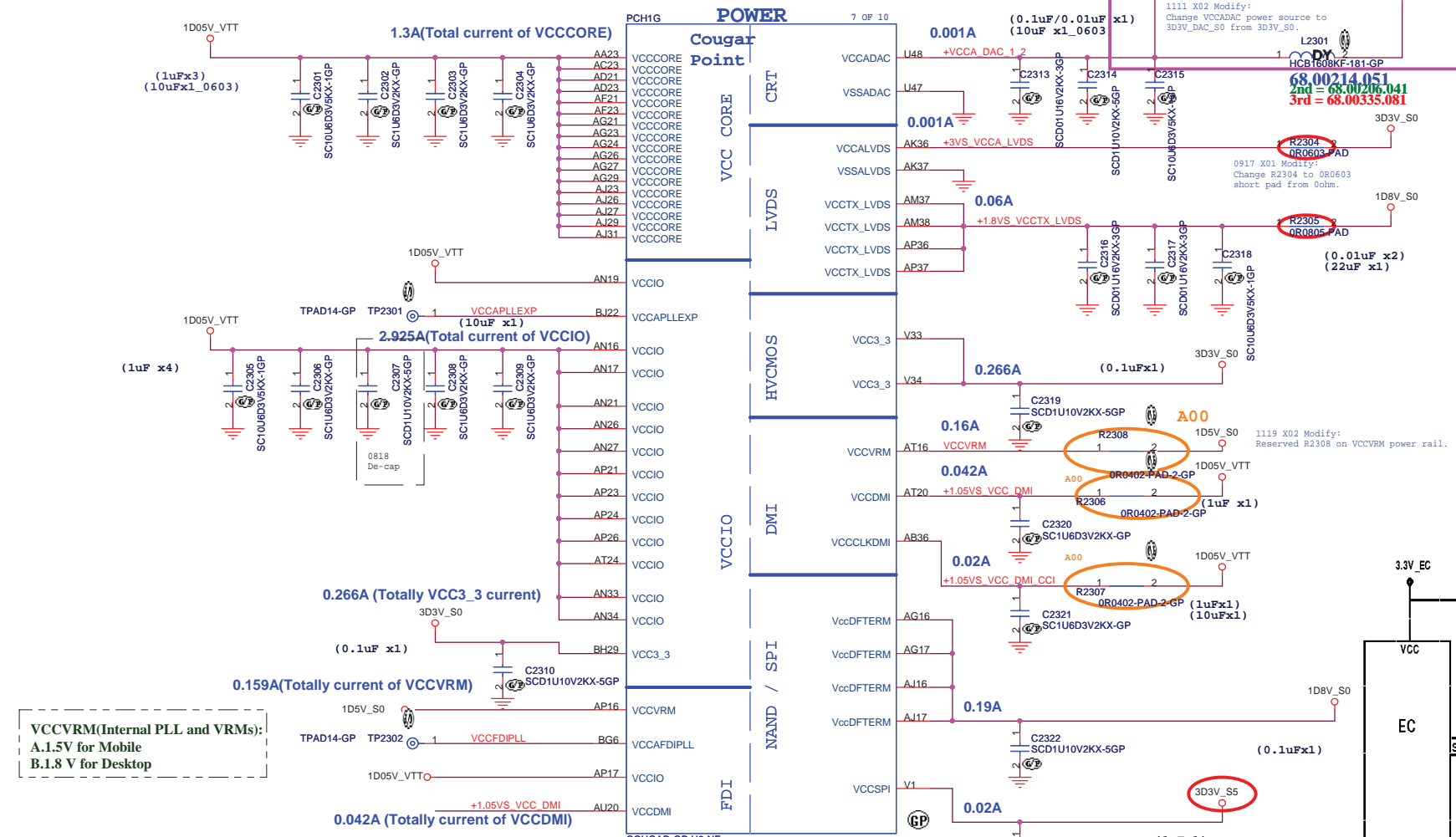






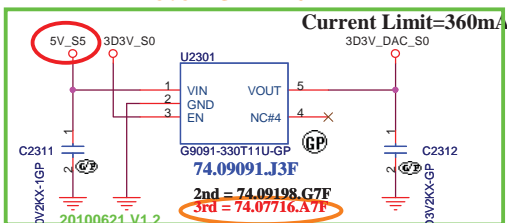






VCCVRM(Internal PLL and VRMs):  
A.1.5V for Mobile  
B.1.8 V for Desktop

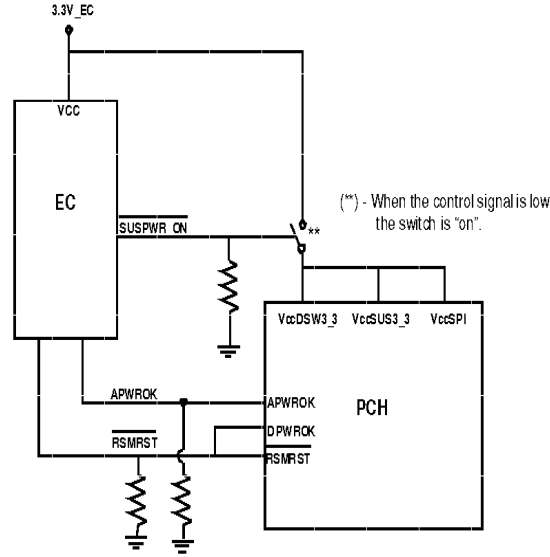
1122 X02 Modify:  
Removed U2302 LDO for VCCVRM.



1117 X02 Modify:  
Add G9091 LDO circuit for CRT DAC power  
to avoid monitor noise issue.  
1122 X02 Modify:  
base on layout condition change 3D3V\_DAC\_S0  
circuit.  
1117 X02 Modify:  
Change U2301 at XBuild batch run config

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

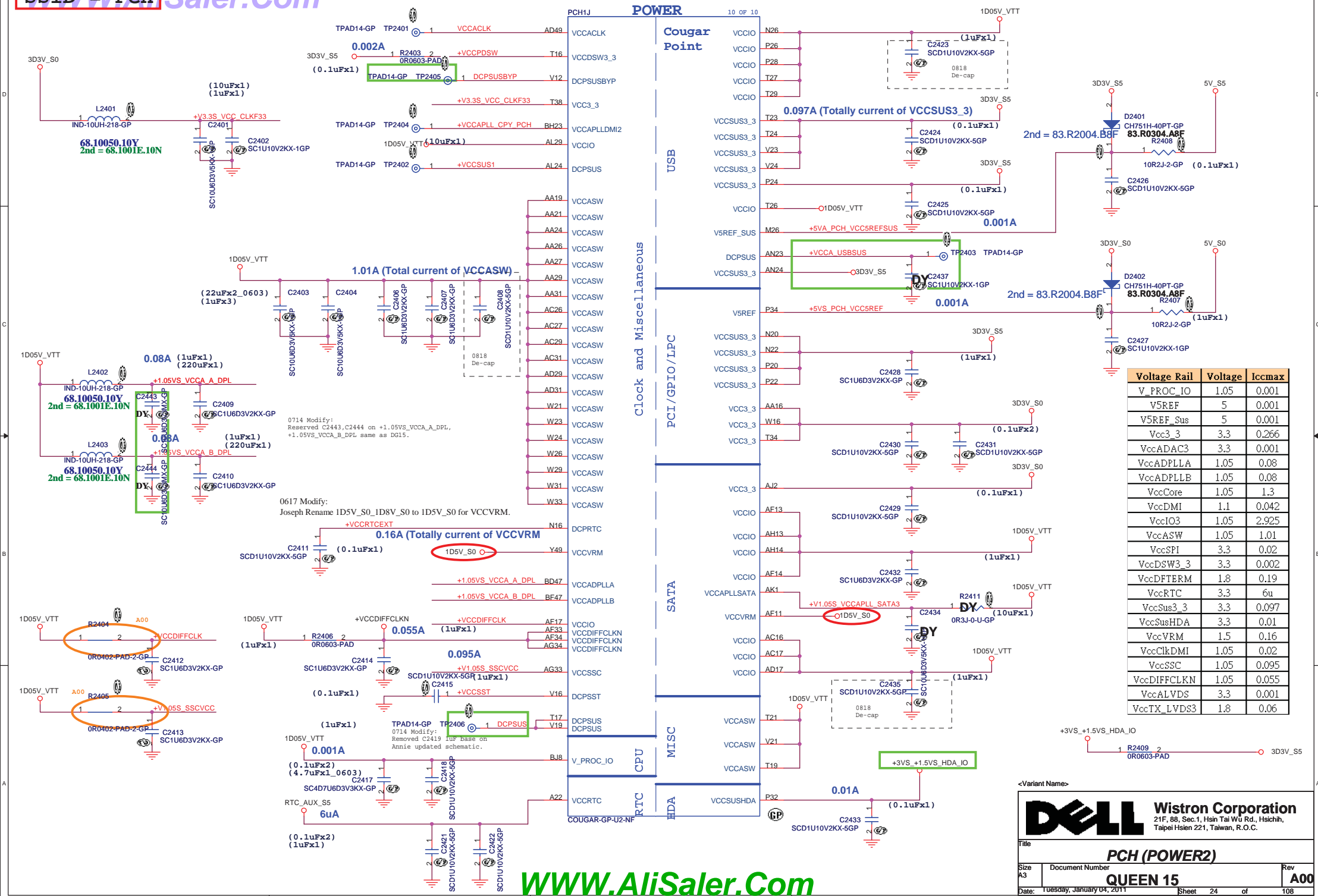
Variant Name: \_\_\_\_\_

**DELL** **Wistron Corporation**

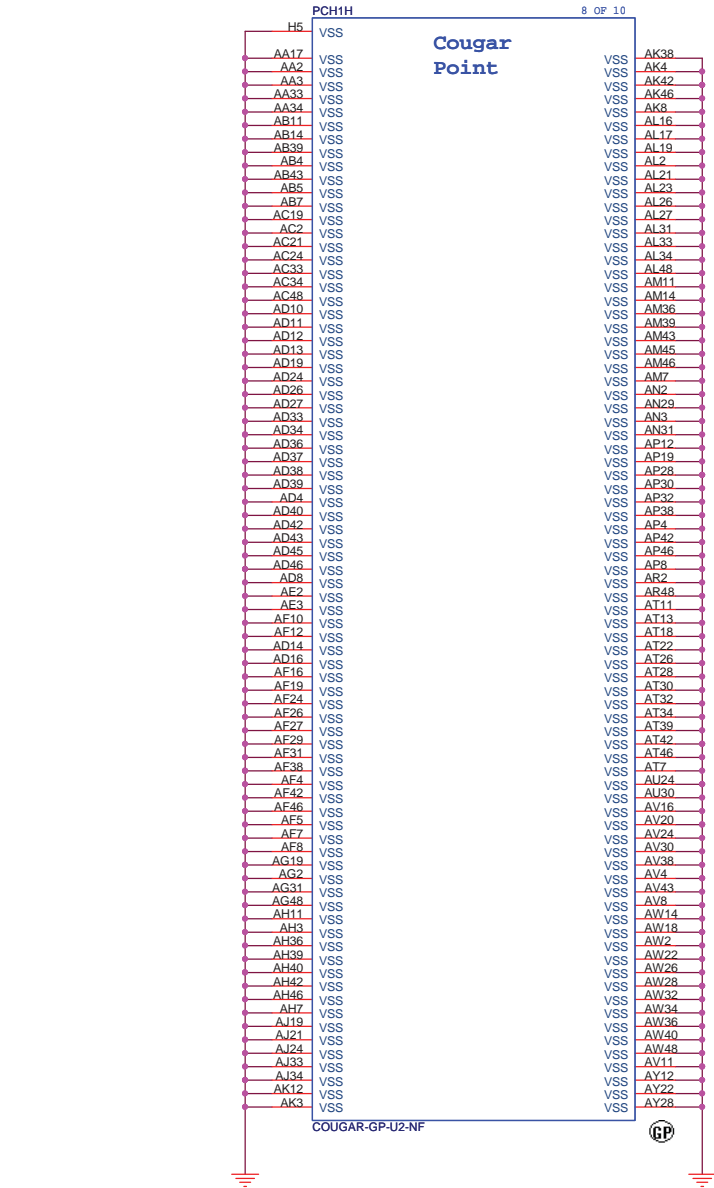
Title: **PCH (POWER1)**

Size: A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet: 23 of 108



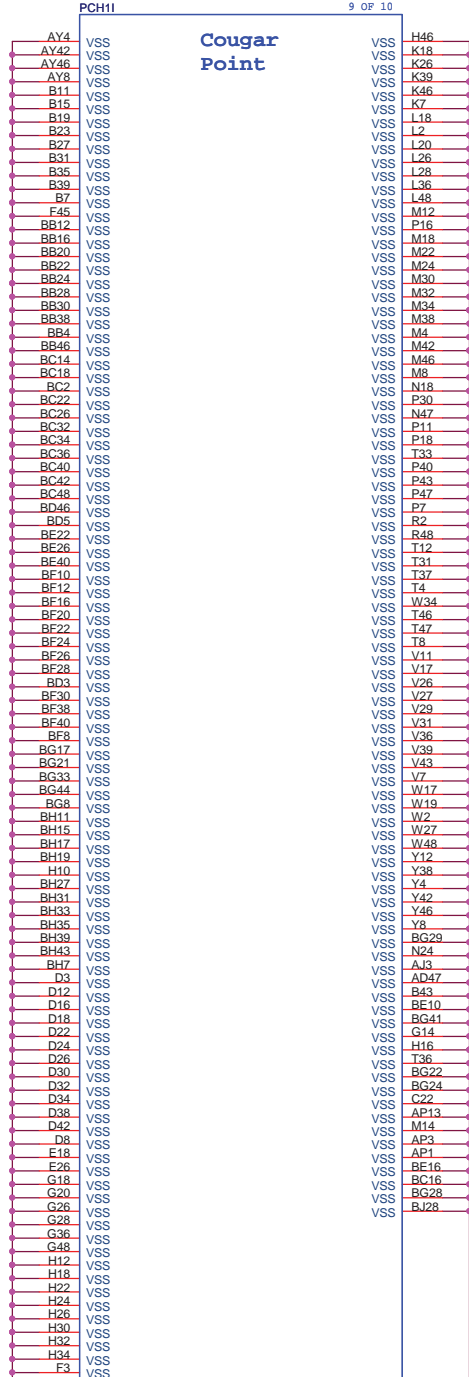
Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06



PCH1H 8 OF 10

Cougar Point

COUGAR-GP-U2-NF



PCH1H 9 OF 10

Cougar Point

COUGAR-GP-U2-NF



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**PCH (VSS)**

Size A3 Document Number **QUEEN 15** Rev **A00**

Date: Tuesday, January 04, 2011 Sheet 25 of 108

( Blanking )

<Variant Name>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

*Reserved*

Size  
A3

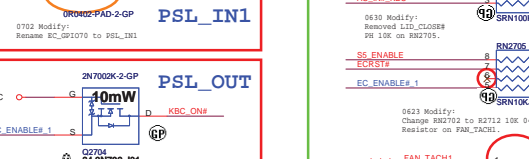
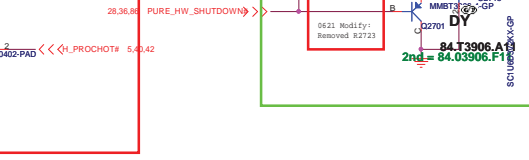
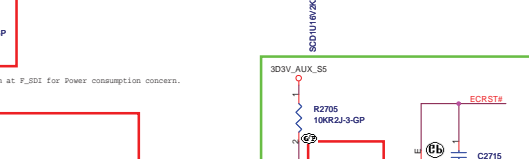
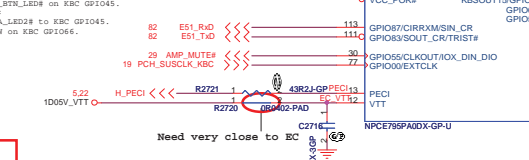
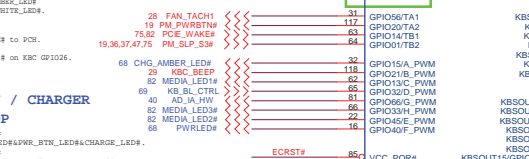
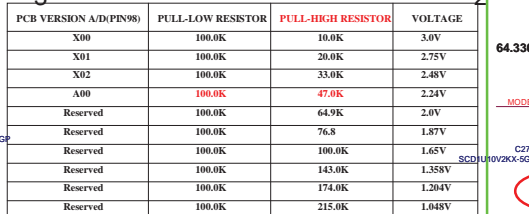
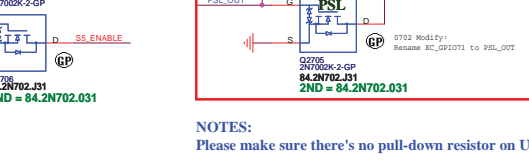
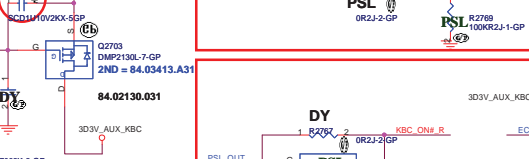
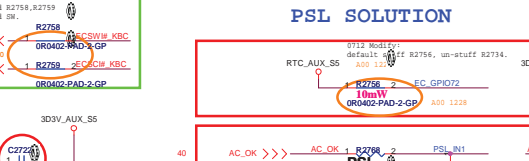
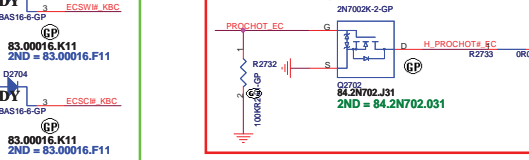
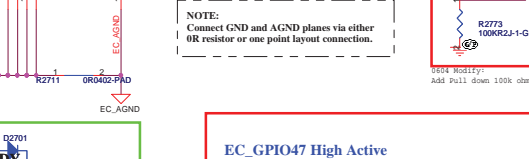
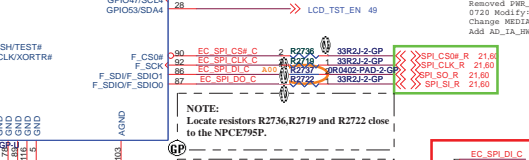
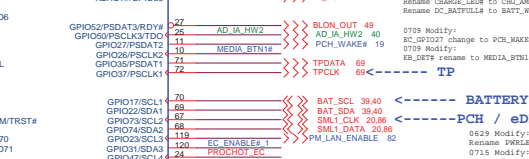
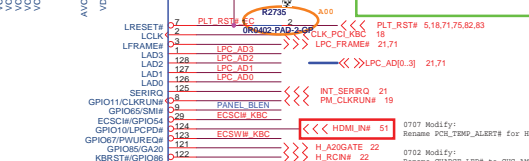
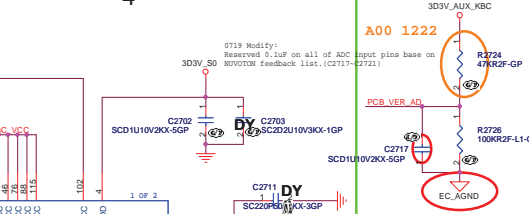
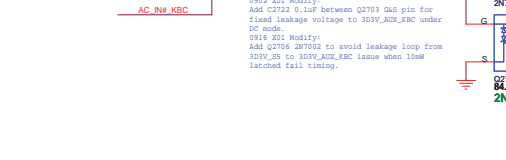
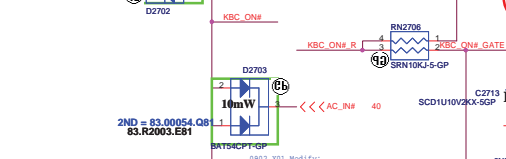
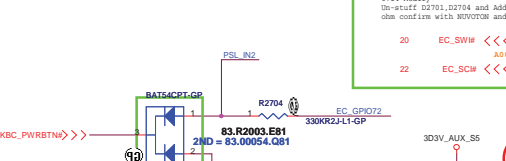
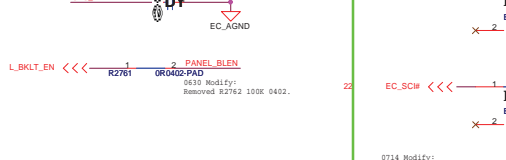
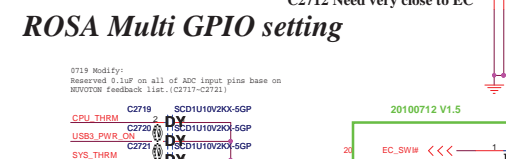
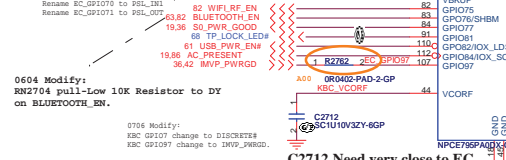
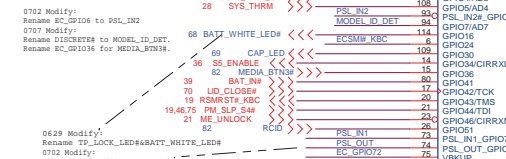
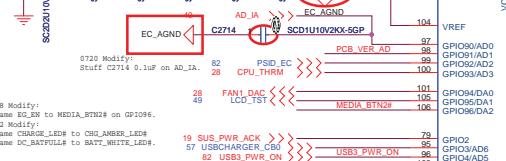
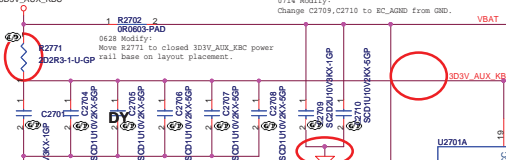
Document Number  
**QUEEN 15**

Date: Tuesday, January 04, 2011

Rev  
**A00**

Sheet 26 of 108

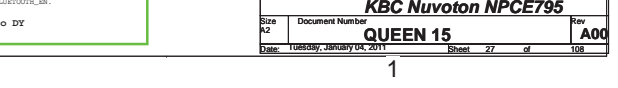
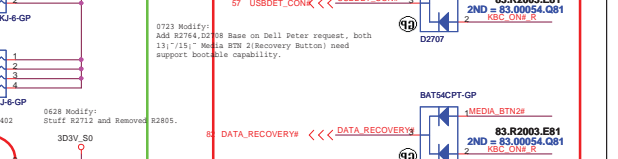
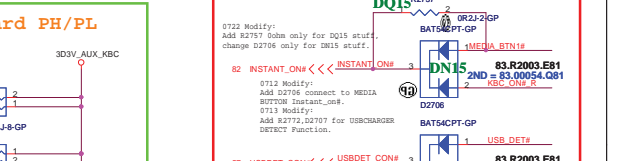
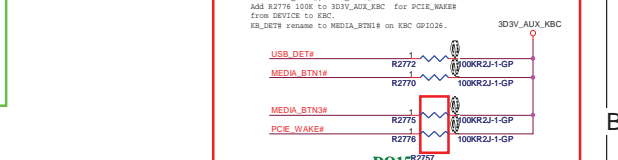
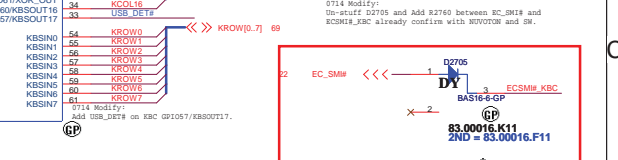
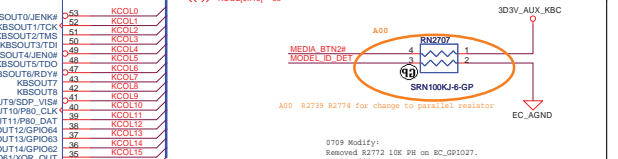




MODEL_ID_DET	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K	3.0V
DQ15_ATI	100.0K	20.0K	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K	2.24V
DN15_ATI	100.0K	64.9K	2.0V
DQ13_ATI	100.0K	76.8K	1.87V
DQ13_ATI	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.38V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

215K=64.21535.6DL

Notes:  
The total SPI interface signal between EC and PCH can't exceed 6500mil. The mismatch between SPI signal must be within 500mil



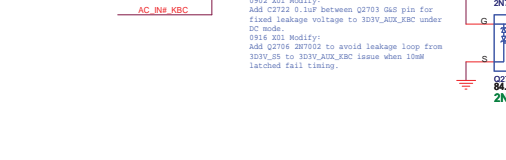
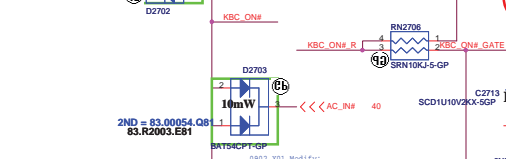
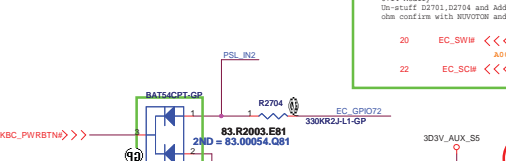
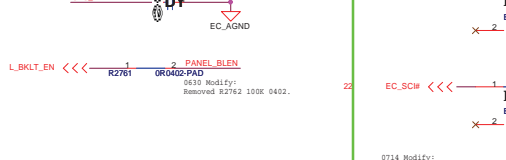
# ROSA Multi GPIO setting

0719 Modify:  
Reserved 0.1uF on all of ADC input pins base on NOVOTON feedback list. (C2717-C2721)

0630 Modify:  
Removed R2762 100K 0402.

0630 Modify:  
Add C2722 0.1uF between Q2703 Gnd pin for fixed leakage voltage to 3D3V\_AUX\_KBC under DC mode.

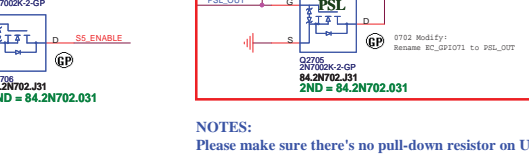
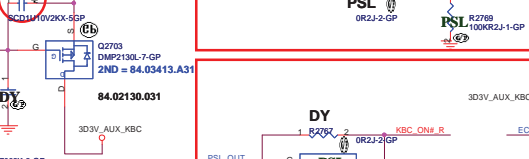
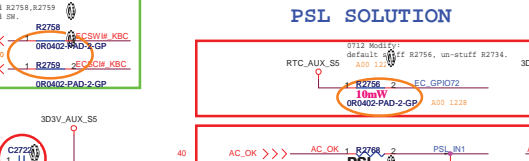
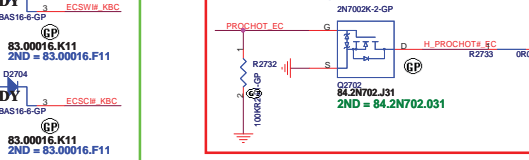
0716 001 Modify:  
Add Q2708 2N7002 to avoid leakage loop from 3D3V\_SS to 3D3V\_AUX\_KBC issue when 10mW latched fail timing.



C2712 Need very close to EC

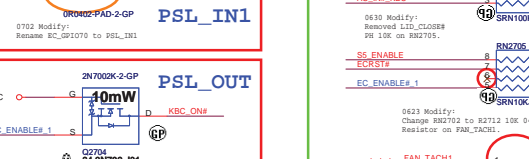
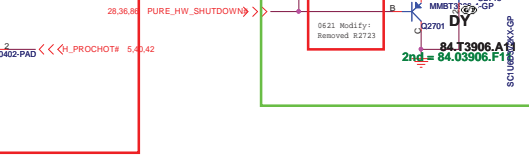
NOTE:  
Locate resistors R2736, R2719 and R2722 close to the NPCE795P.

NOTE:  
Connect GND and AGND planes via either 0R resistor or one point layout connection.



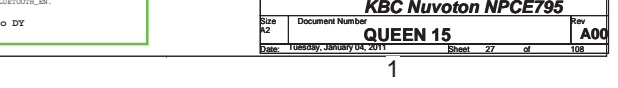
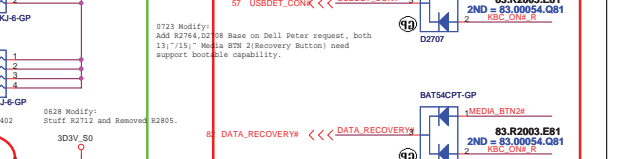
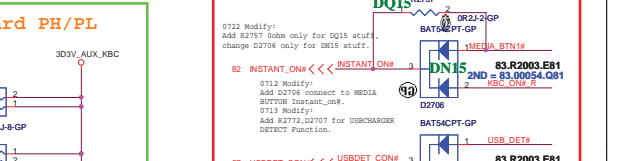
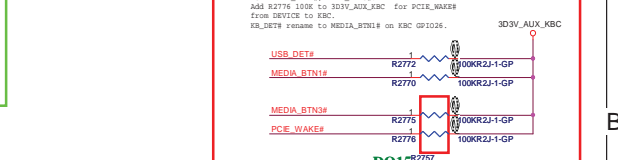
Need very close to EC

0634 Modify:  
Add Pull down 100k ohm at P\_SDI for Power consumption concern.



0709 Modify:  
Removed R2772 10K PR on EC\_GP1027.

0714 Modify:  
Un-stuff D2705 and Add R2760 between EC\_RN18 and R20N18\_KBC already confirm with NOVOTON and SH.



NOTES:  
Please make sure there's no pull-down resistor on USB\_PWR\_EN, AC\_PRESENT, ES1\_TXD.

NOTES:  
Please make sure there's no pull-down resistor on USB\_PWR\_EN, AC\_PRESENT, ES1\_TXD.

NOTES:  
Please make sure there's no pull-down resistor on USB\_PWR\_EN, AC\_PRESENT, ES1\_TXD.

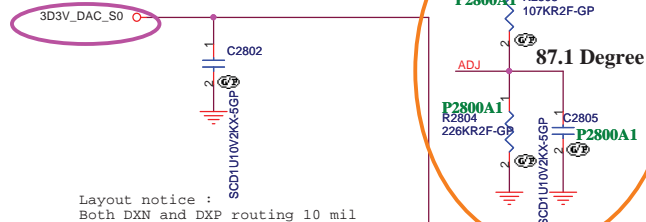
NOTES:  
Please make sure there's no pull-down resistor on USB\_PWR\_EN, AC\_PRESENT, ES1\_TXD.

# Thermal sensor P2800

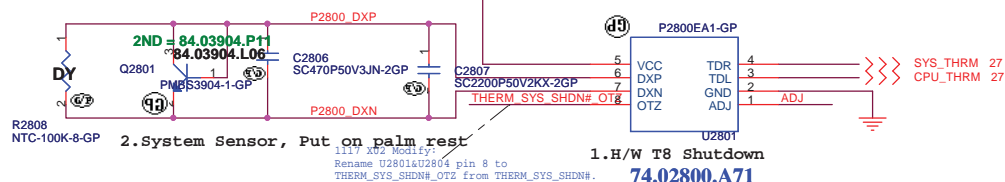
0705 Modify:  
R2802 change to 0ohm 0402 from short pad and default un-stuff.

# Fan controller P2793

1119 X02 Modify:  
Change U2801,U2804,U2805 VCC power to 3D3V\_DAC\_S0 from 3D3V\_S0.



Layout notice :  
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



1.H/W T8 Shutdown  
74.02800.A71

## ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

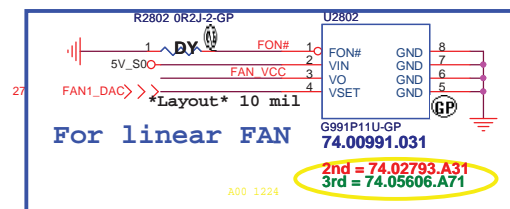
A00 1228 Cancel VGA Thermal sensor P2800 circuit

	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

A00 1227

1111 X02 Modify:  
ADJ&ADJ\_VGA power source change to 3D3V\_DAC\_S0 from 3D3V\_S0 to solve T8 shut down issue.

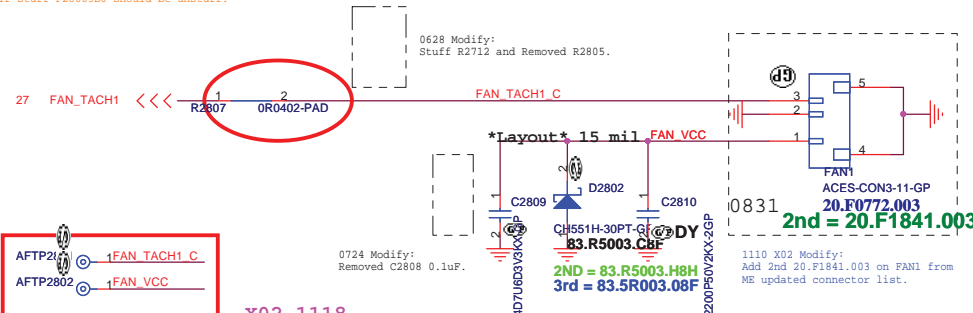
1227 A00 Modify:  
If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.



For linear FAN

2nd = 74.02793.A31  
3rd = 74.05606.A71

0614 Modify:  
Change FAN1 connector part number to 20.D0210.103 base on ME EMN and DXF.  
0712 Modify:  
Change FAN1 part number to 20.F1639.004 from 20.D0210.103 base on latest EMN and DXF.



0724 Modify:  
Removed C2808 0.1uF.

X02 1118

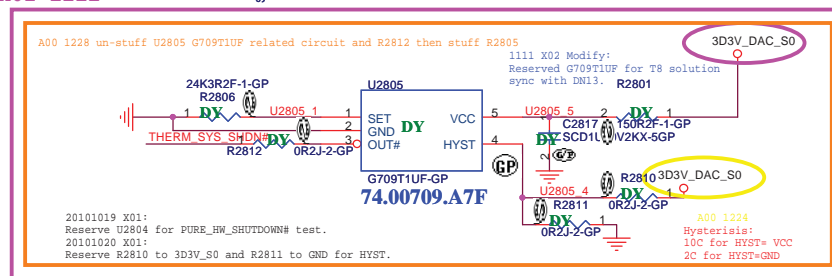
1117 X02 Modify:  
Add R2805 0hm between THERM\_S\_S\_SHDN#\_OTZ and THERM\_S\_S\_SHDN#.

27,36,86 PURE\_HW\_SHUTDOWN# <<<

## EMI/ESD



X02 1111



1111 X02 Modify:  
ADJ&ADJ\_VGA power source change to 3D3V\_DAC\_S0 from 3D3V\_S0 to solve T8 shut down issue.

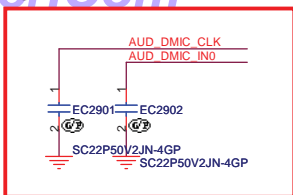
<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

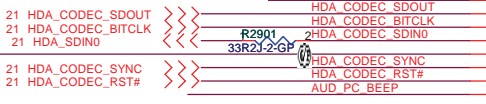
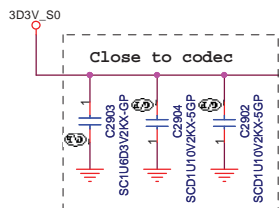
Title	Document Number	Rev
Thermal P2800/Fan Controller P2793	QUEEN 15	A00
Date: Tuesday, January 04, 2011	Sheet 28 of 108	

SSID = AUDIO

For EMI

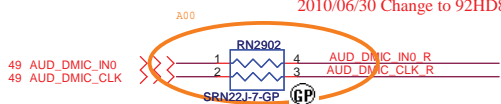


1122 X02 Modify:  
change R2920, R2921 to 22ohm from 0ohm and  
stuff R2901, EC2902 22p from EMC Neo updated.

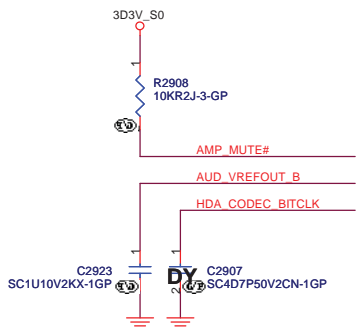


0707 Modify:  
updated U2901 part number from data base.

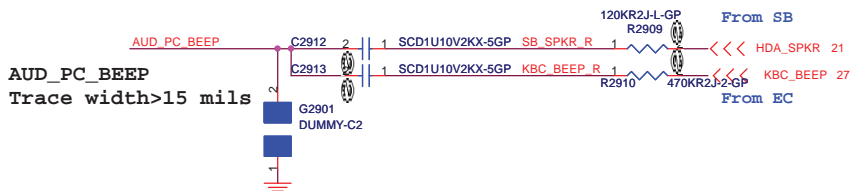
2010/06/30 Change to 92HD87 (71.92H87.A03)



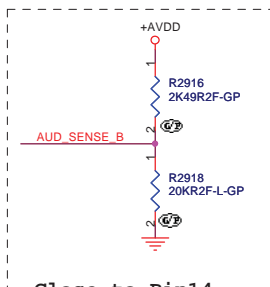
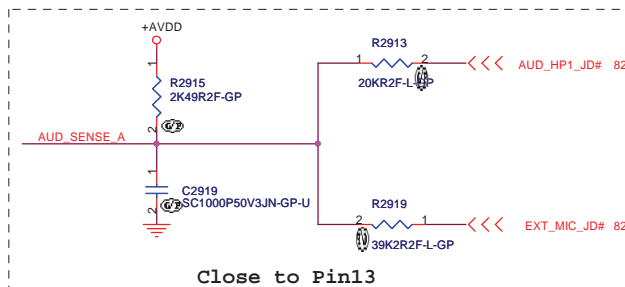
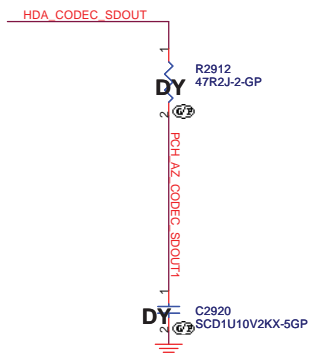
20101220 R2920 R2921 for change to parallel resistor



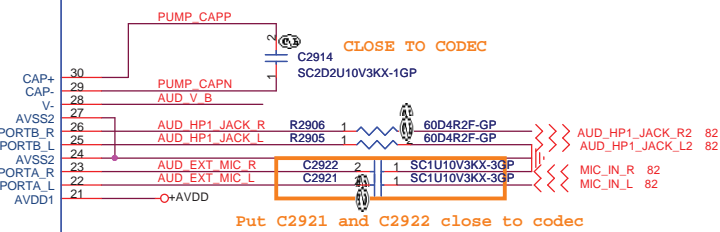
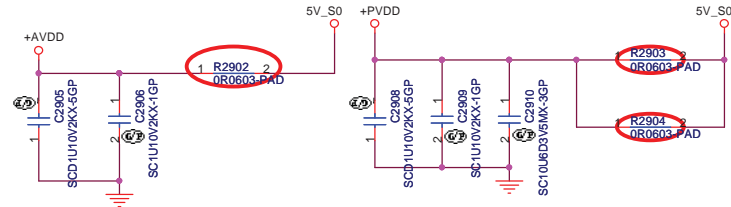
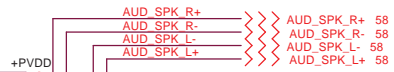
AUD\_PC\_BEEP  
Trace width>15 mils



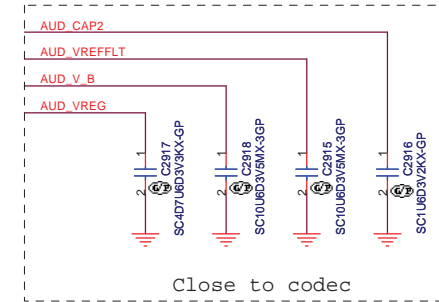
Azalia I/F EMI



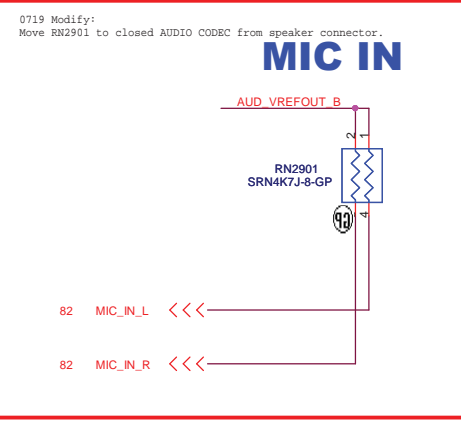
WWW.AliSaler.Com



Put C2921 and C2922 close to codec




Close to codec



<Core Design>

(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Tuesday, January 04, 2011	Sheet 30 of 108
---------------------------------	-----------------

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A3

Document Number  
**QUEEN 15**

Date: Tuesday, January 04, 2011

Rev  
**A00**

Sheet 31 of 108

48MHz clock input trace of characteristic impedance ( $Z_0$ ) must be 50  $\pm$  15%.

20 CLK\_PCH\_48M >>>—

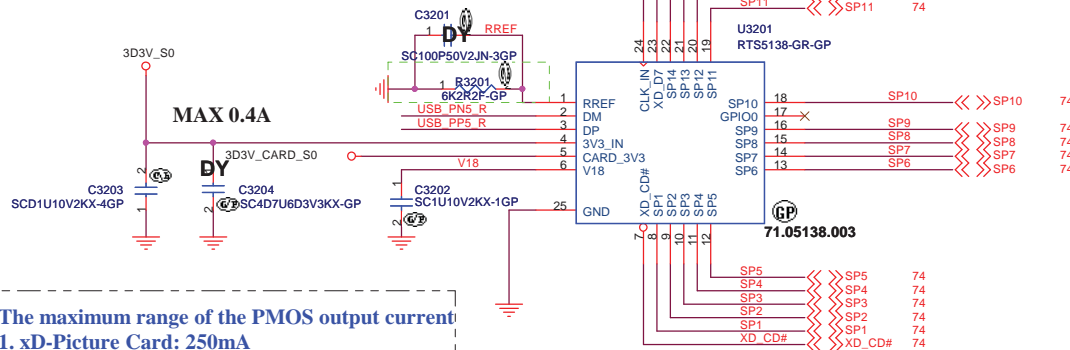
3D3V\_CARD\_S0

3D3V\_CARD\_S0

C3206  
SCD1U10V2KX-4GP

C3207  
SC4D7U6D3V3KX-G

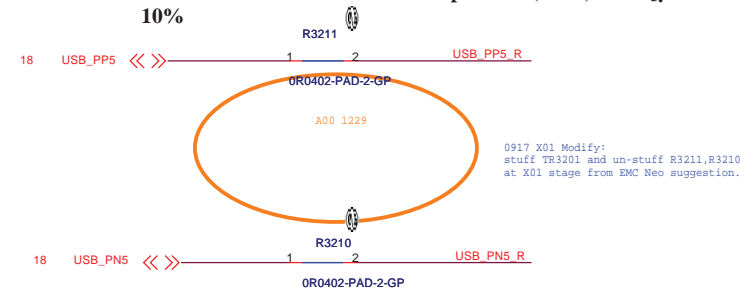
Close to chip



1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

- 1.RTS5138: pin 4 (3V3\_IN) trace fixed width is 30 mils (minimum).
- 2.RTS5138: pin 5 (CARD\_3V3) trace fixed width is 30 mils (minimum).
- 3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).  
Keep the trace routing lengths as short as possible.
- 4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
- 5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
- 6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
- 7.It is recommended that use of ferrites bead on power trace.
- 8.Via size: Pad>=32 mils, Finished hole>=16 mils.

**The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance ( $Z_{diff}$ ) is 90Ω±10%**




**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>Card Reader-RTS5138</b>			
Size A3	Document Number	Rev	
	<b>QUEEN 15</b>	<b>A00</b>	
Date:	Tuesday, January 04, 2011	Sheet 32 of	108



(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 33 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 34 of	108

( Blanking )

<Core Design>



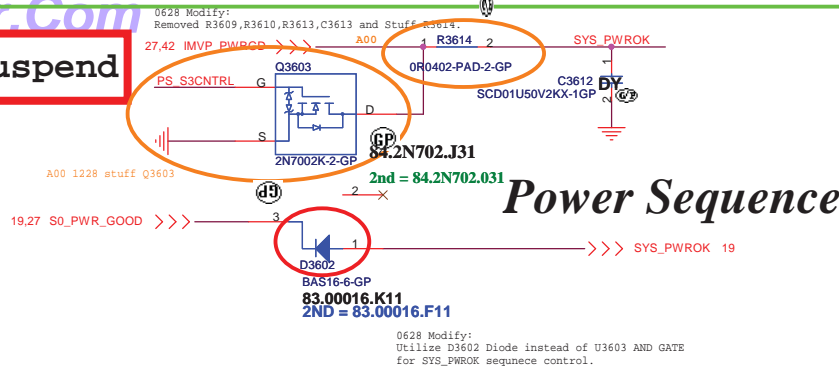
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

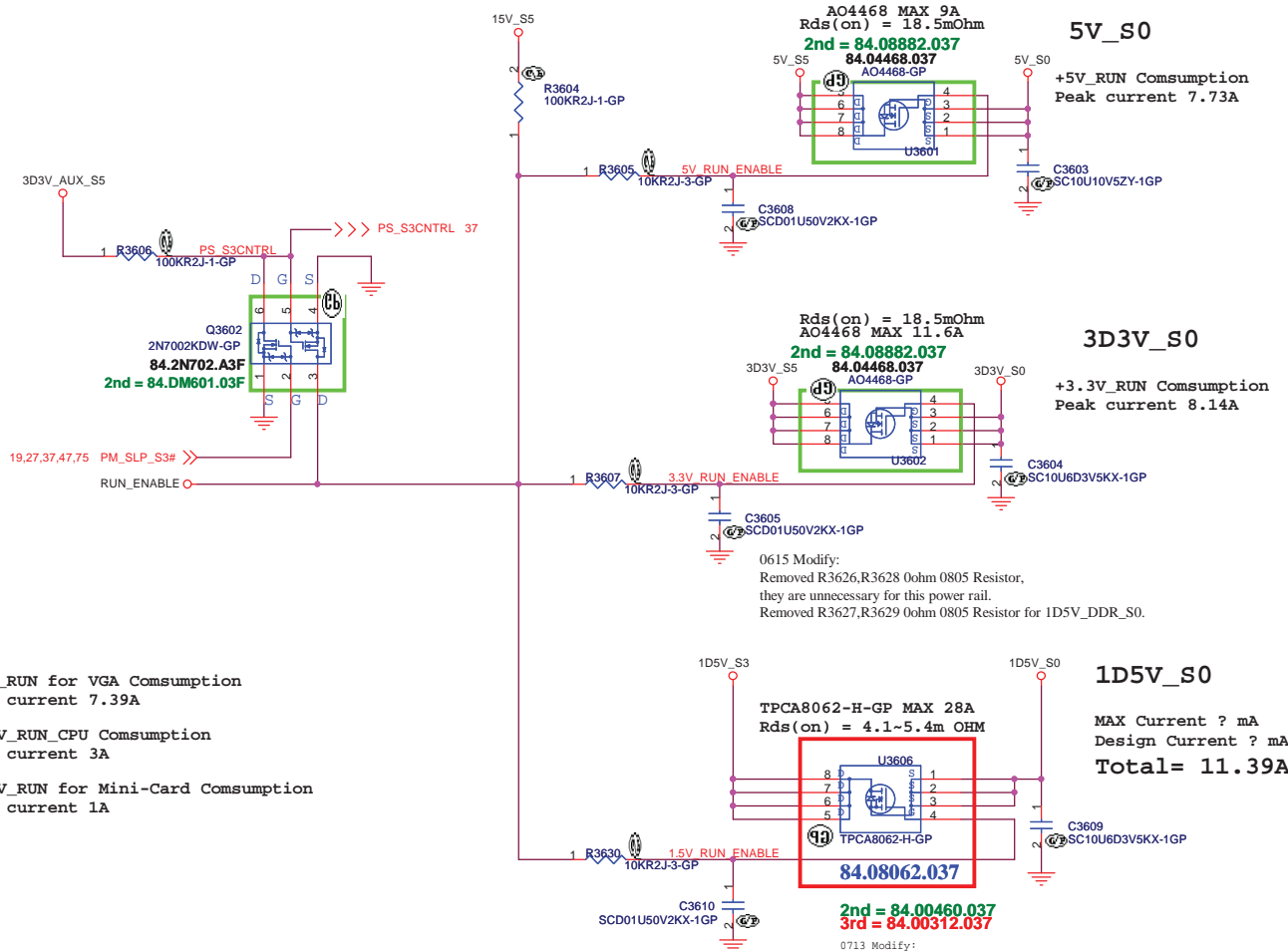
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 35 of	108

SSID = Reset.Suspend



## Power Sequence

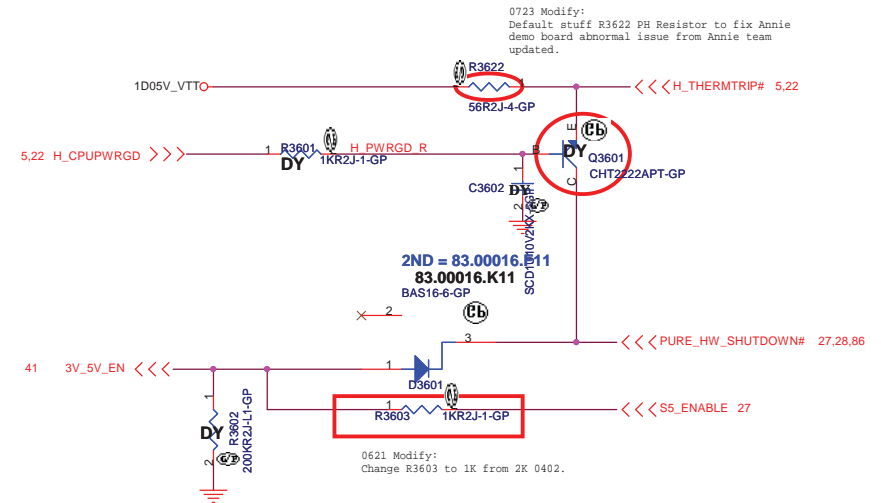
## ROSA Run Power



1.5V\_RUN for VGA Consumption  
Peak current 7.39A

+1.5V\_RUN\_CPU Consumption  
Peak current 3A

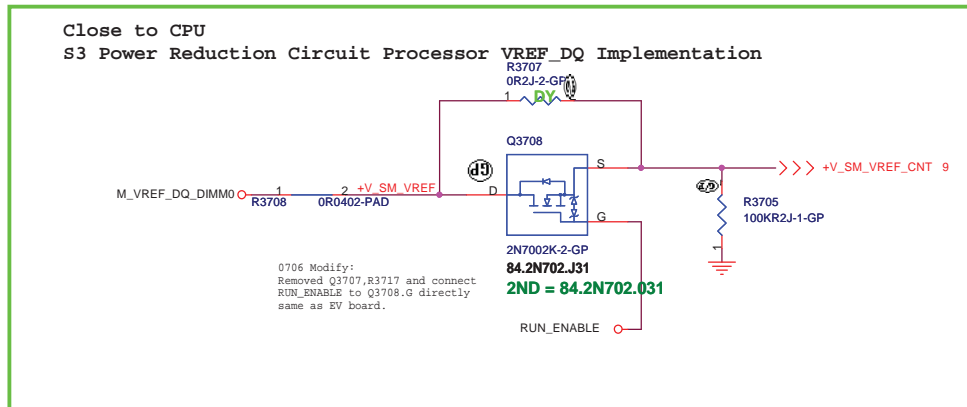
+1.5V\_RUN for Mini-Card Consumption  
Peak current 1A



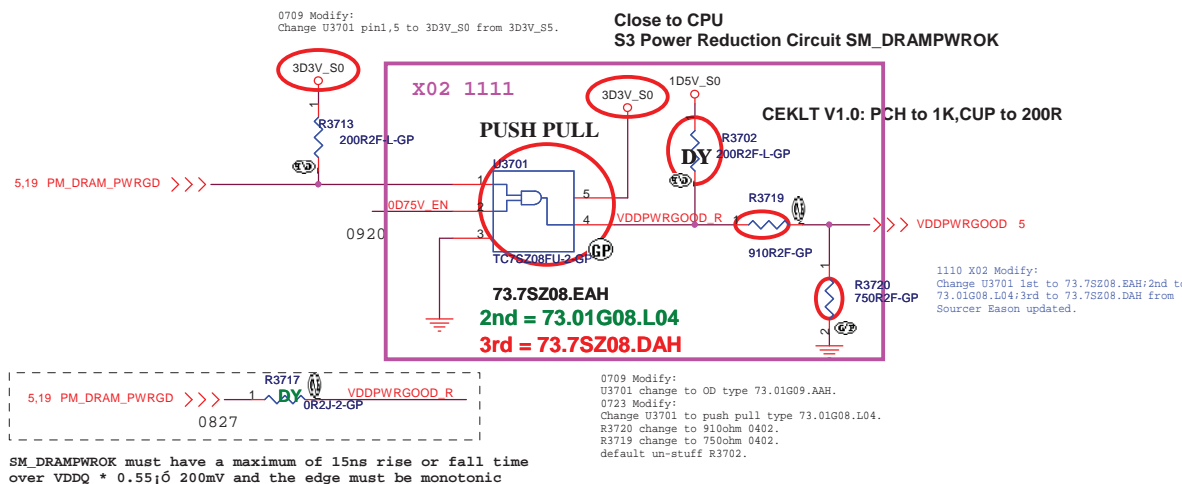
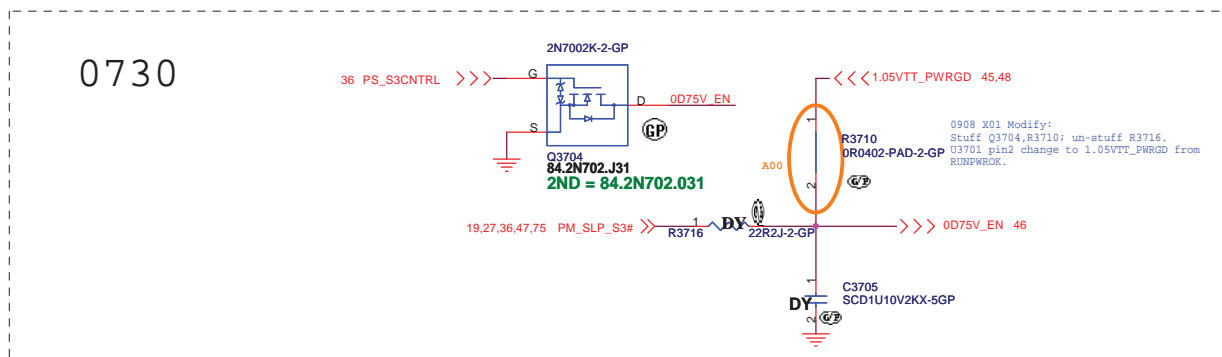
0719 Modify:  
Reserved EC3601 0.1uF near  
C3604 for EMC NEO suggestion.

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Power Plane Enable</i></b>			
Size A3	Document Number <b>QUEEN 15</b>		Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 36	of 108	

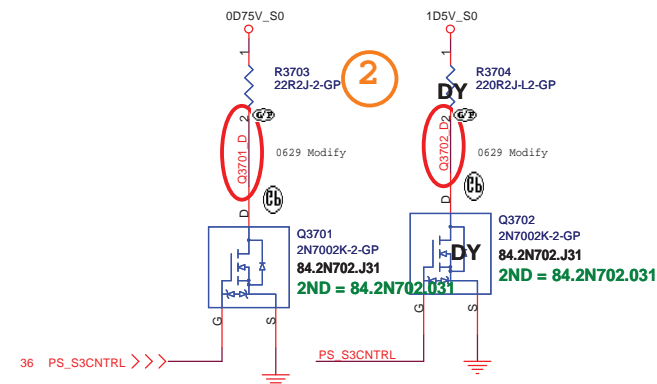


5 S3 Power Reduction X01 20091111

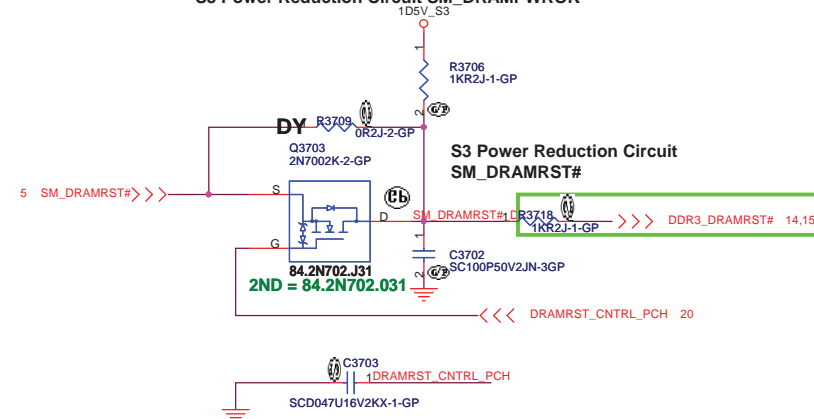


SM\_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55; 200mV and the edge must be monotonic

**Close to DIMM**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



**Close to CPU**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



DN15ATI


**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			ADAPTER		
Size	Document Number		QUEEN 15		Rev
A3					A00
Date:	Tuesday, January 04, 2011		Sheet	37	of 108

SSID = PWR.Support

(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

QUEEN 15

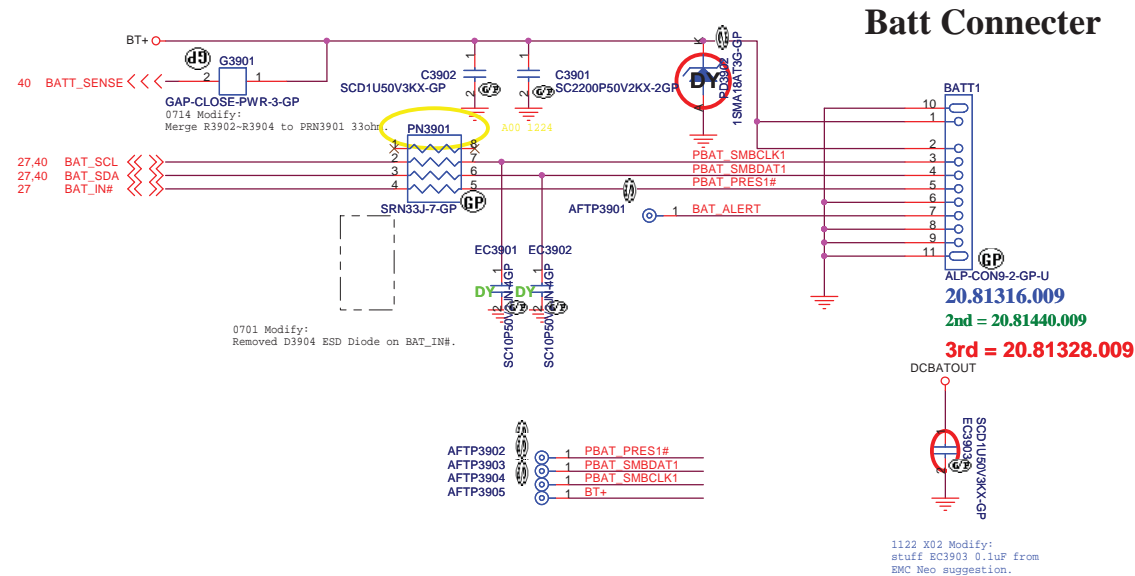
Rev

A00

Date: Tuesday, January 04, 2011

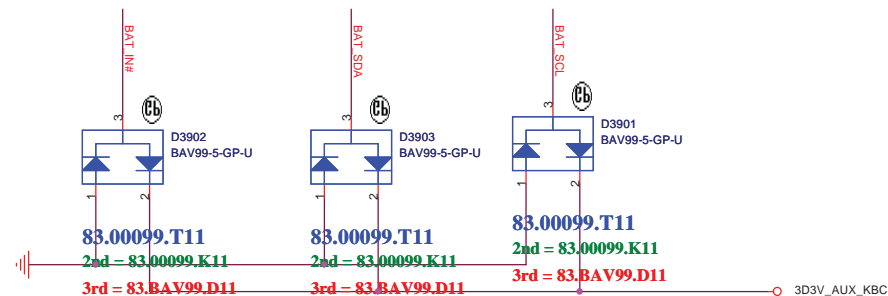
Sheet 38 of 108





For actual location, need to be swap all pin

Close to Batt Connector



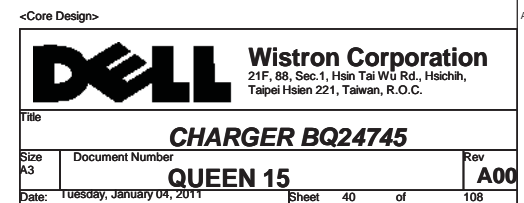
0930 X01 Modify:  
Change D3901-D3903 main source to 83.00099.T11  
for 83.BAV99.D11 shortage issue.

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

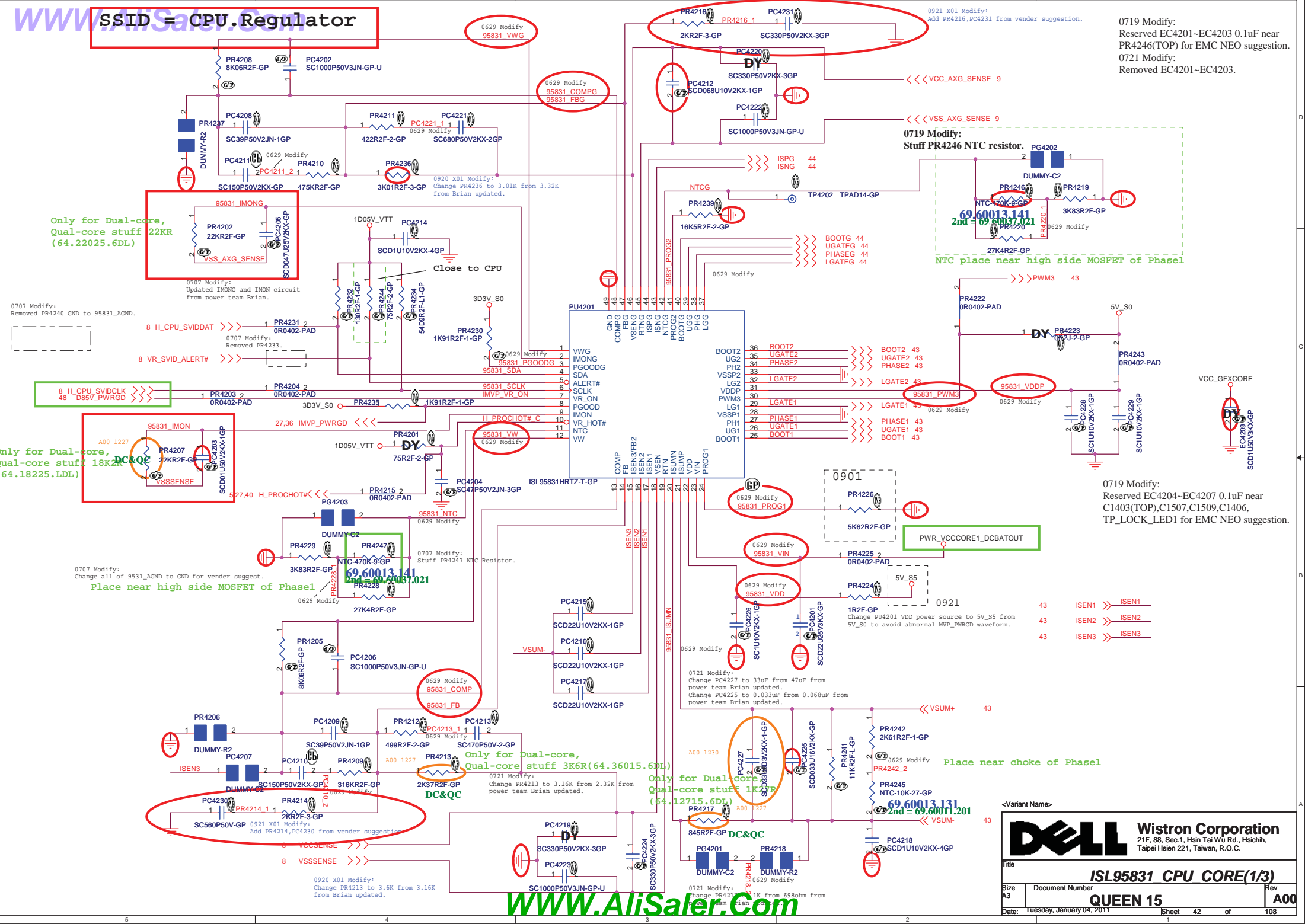
Title				<b>BATT CONN</b>	
Size	Document Number			Rev	
A3	<b>QUEEN 15</b>			<b>A00</b>	
Date:	Tuesday, January 04, 2011	Sheet	39	of	108

0719 Modify:  
Reserved EC4007 0.1uF near PG4006  
for EMC NEO suggestion.





SSID = CPU.Regulator



**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95831 CPU CORE(1/3)**

Size: A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet: 42 of 108

84.00462.037  
SIR462DP  
Id=30A, Qg=8.8nC,  
Rdson=7.9~10 mohm

0719 Modify:  
Change PU4308 part number to 84.00172.037 from  
84.07686.037 base on power team Brian suggestion.  
0726 Modify:  
Brian updated PU4308 change to 84.00462.037.

80.3371V.A2L  
330uF, 2.5V, B2  
ESR=9mΩ, Iripple=3.073A

68.R3610.20A  
0.36uH, Idc=20A,  
Isat=25A  
DCR=1.4 +/-7% mohm

Vcc\_core  
Iomax=53A  
OCP>97.5A

84.00460.037  
SIR460DP  
Id=40A, Qg=16.8nC,  
Rdson=4.7~6.1mohm

## FOR NVIDIA VENTURA

0708 Modify:  
PR4320 change to BIG SIZE footprint for CPU VENTURA.  
0705 Modify:  
R4346 change to PR4320 4m ohm sense  
Resistor from 3m ohm.  
0705 Modify:  
Removed R4347 sense Resistor base on VENTURA SPEC.

0705 Modify:  
Add PR4321, PR4322, PC4319.

0702 Modify:  
Change U4306 power source to  
3D3V\_VGA\_S0 from 3D3V\_S0.

0712 Modify:  
Change VENTURA solution part number to  
74.00900.079 from 74.00219.079.

0719 Modify:  
Reserved PTC4307 47uF.  
0721 Modify:  
Removed PTC4307.

DN15AT1

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

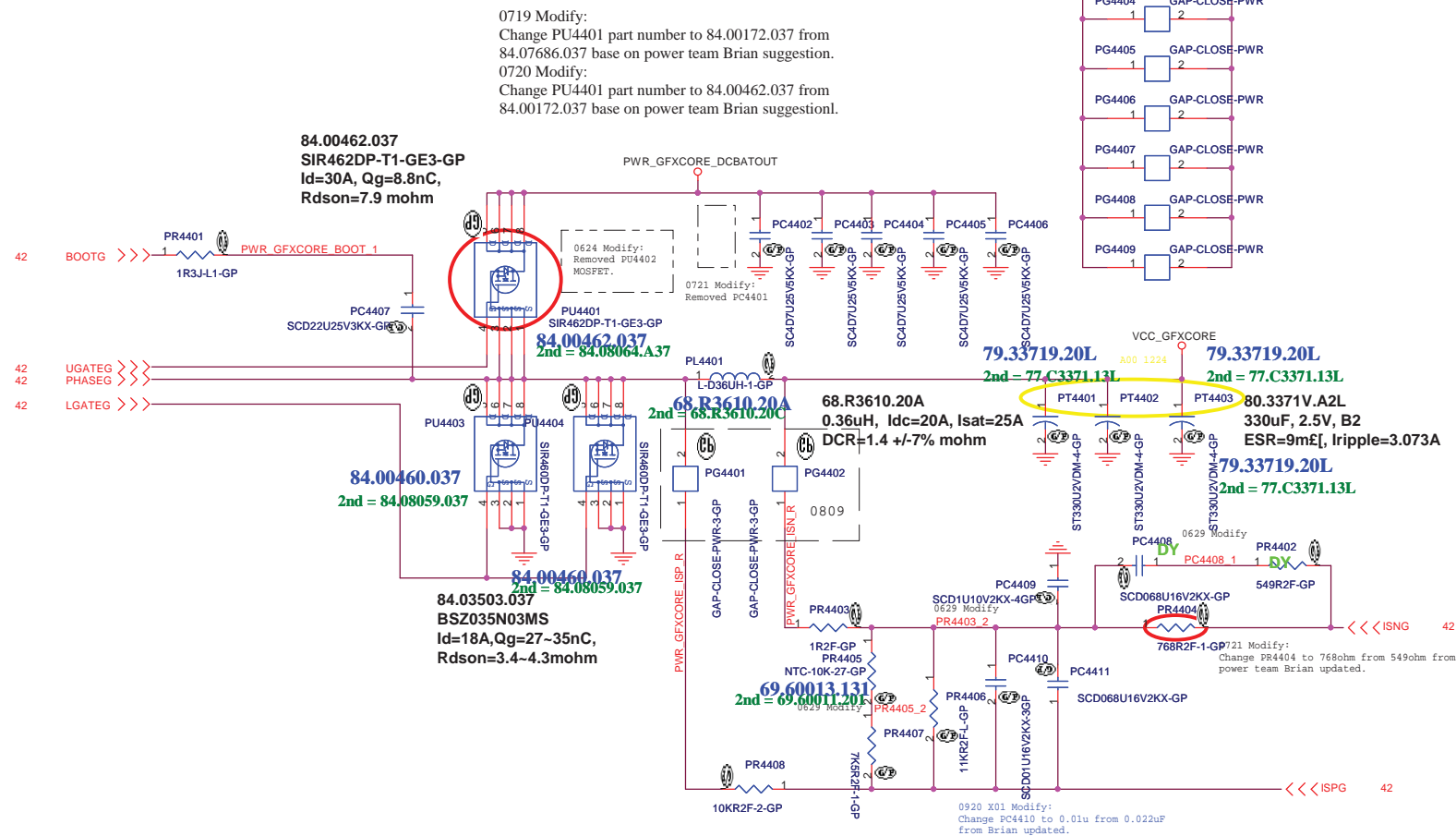
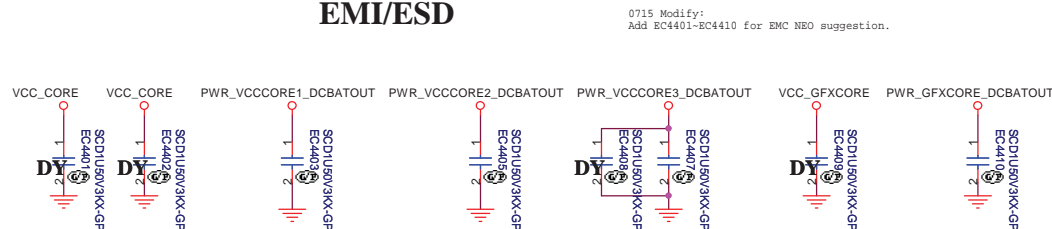
Title  
**ISL95831 CPU CORE (2 of 3)**

Size Document Number  
**QUEEN 15**

Date: Tuesday, January 04, 2011 Sheet 43 of 108

Would be instead of INA219 by HPA00900

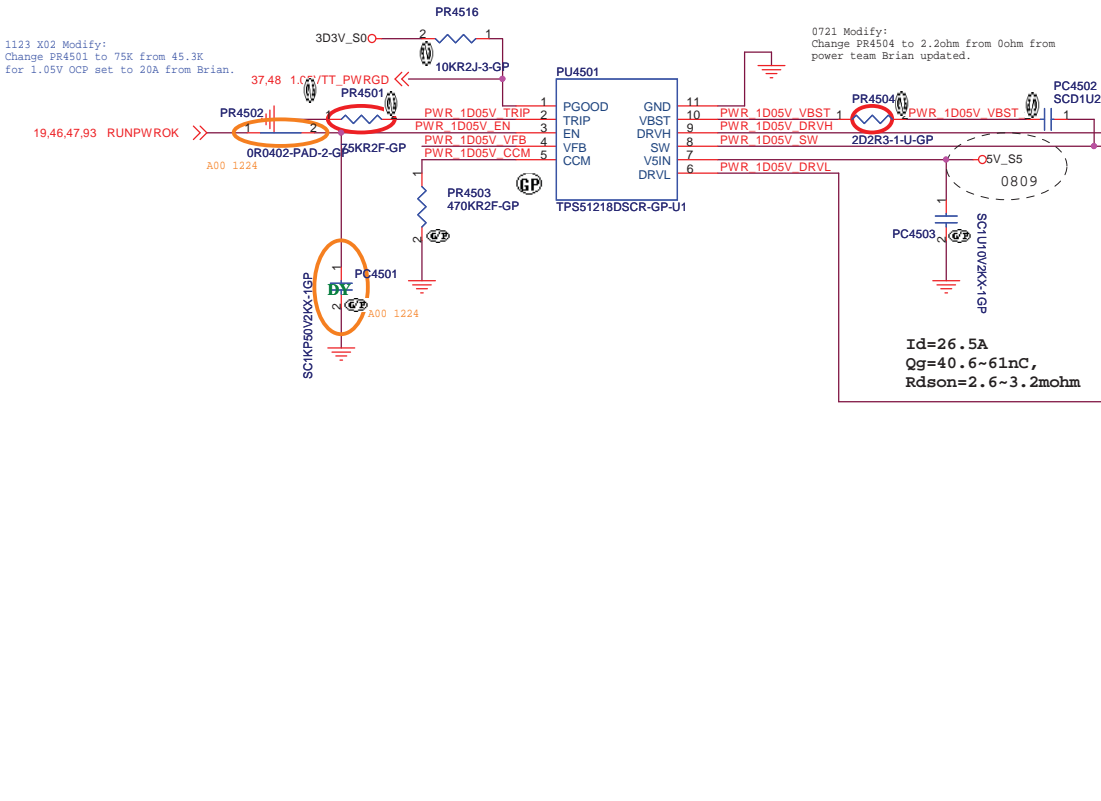


**EMI/ESD**



# TPS51218 for 1D05V

1123 X02 Modify:  
Change PR4501 to 75K from 45.3K  
for 1.05V OCP set to 20A from Brian.



DN15ATI

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			TPS51218 +1.05V VTT		
Size	Document Number		Rev		
A3	QUEEN 15		A00		
Date:	Tuesday, January 04, 2011		Sheet	45	of 108

SSSID = PWR.Plane.Regulator 1p5v0p75v

0719 Modify:  
Change PU4602 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.

84.00172.037  
BSZ115N03MSC  
Id=20A, Qg=9.8nC,  
Rdson=8.9 mohm

0630 modify  
PU4602  
SIR172DP-T1-GE3-GP  
84.00172.037  
2nd = 84.08065.037

84.00460.037  
SIR460DP-T1-GE3  
Id=40A, Qg=16.8nC,  
Rdson=4.7~6.1 mohm

84.00460.037  
2nd = 84.08059.037

0913 X01 Modify:  
Add 2nd source 68.R681A.10Q on PL4601  
base on Brian updated 2nd source excel file.

PL4601  
IND-D68UH-51-GP-U  
68.R6810.20G  
2nd = 68.R681A.10Q  
68.R6810.20G  
Id=22~39A  
DCR=2.4~2.7mohm  
Size=10X11.5X4

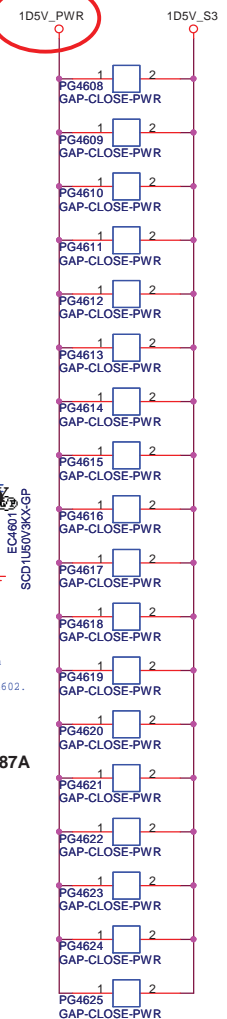
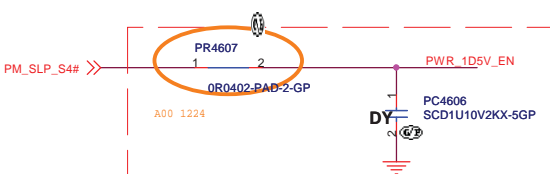
Design Current = 14.45A  
22.71A<OCP< 26.84A

79.3971V.30L  
2nd = 77.93971.02L

0902 X01 Modify:  
Change PTC4602 to 79.3971V.30L from 79.22719.20L sync with DQ15-NV  
Add 2nd source 77.93971.02L on PTC4602.

79.3971V.30L  
390uF, 2.5V, 6.3X5.7  
ESR=10mΩ, Iripple=3.87A

0721 Modify:  
Removed PR4615, PR4616 and connect 0D75V\_EN to VTTEN directly.



0721 Modify:  
Removed PR4615, PR4616 and connect 0D75V\_EN to VTTEN directly.

0721 Modify:  
Change PR4602 to 68K from 6.2K from power team Brian updated.

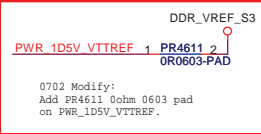
0920 X01 Modify:  
Change PR4602 to 110K from 68K from Brian updated.

0630 Modify:  
Change 1D5V power solution to TPS51216 from TPS5116 follow power team Brian suggest.

0630 Modify:  
Change PC4610 to 0.22u 0402 from 0603 from Brian.

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR5003	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



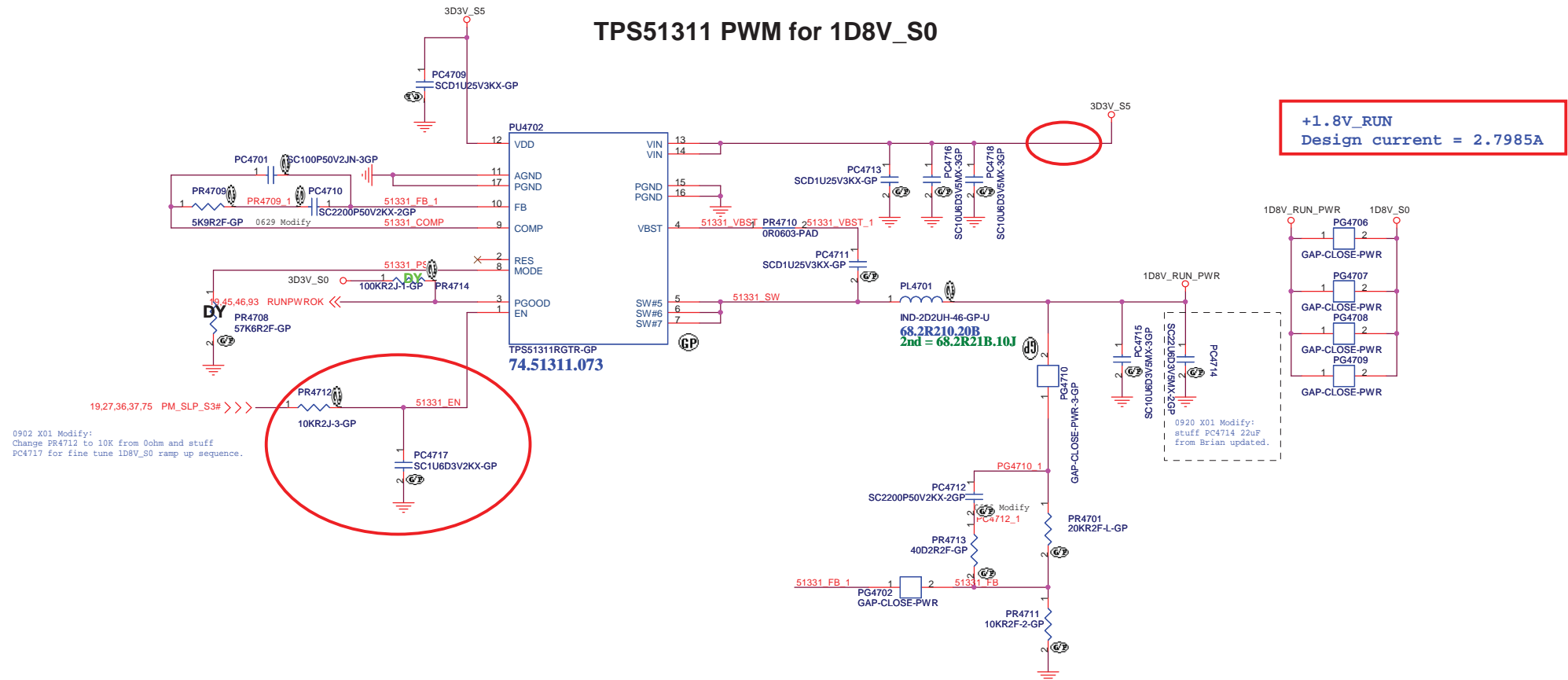
0702 Modify:  
Add PR4611 0ohm 0603 pad on PWR\_1D5V\_VTTREF.

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title: <b>TPS51116 +1.5V SUS</b>	
Size A3	Document Number	Rev A00	
Date: Tuesday, January 04, 2011	Sheet 46	of	108

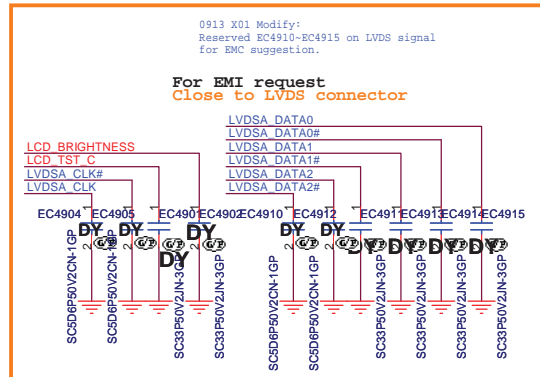
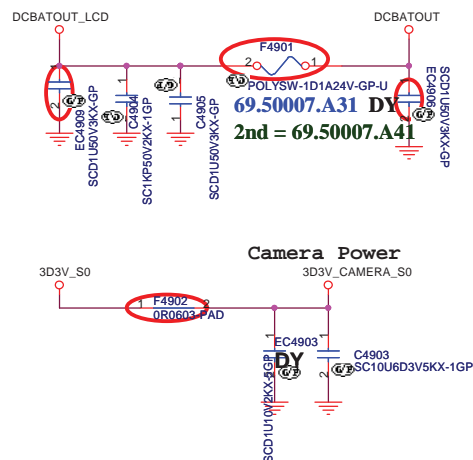
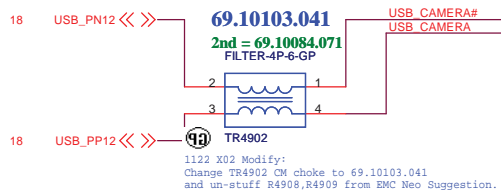
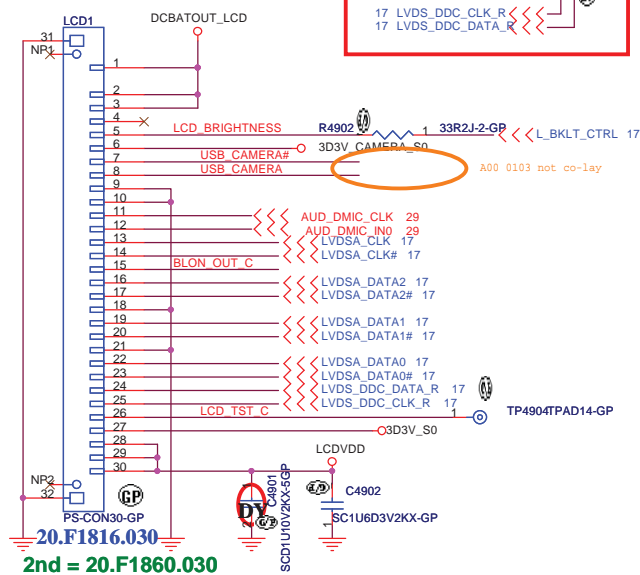
WWW.AliSaler.Com

## TPS51311 PWM for 1D8V\_S0



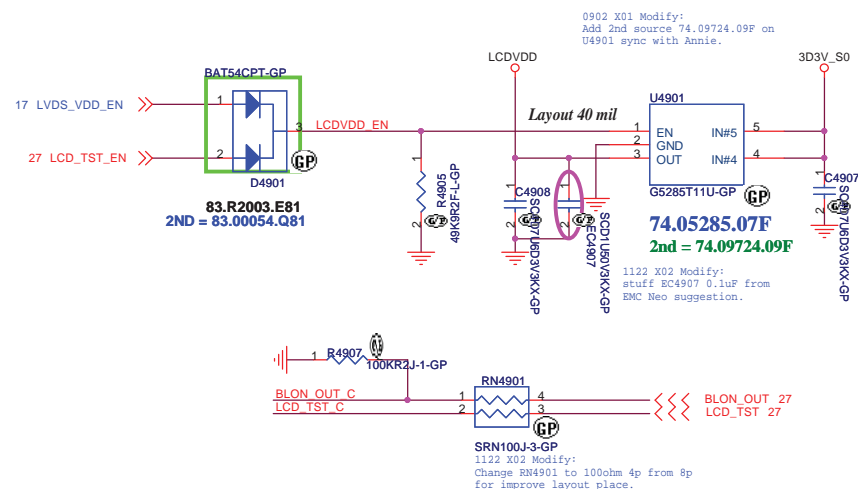


## LVDS CONNECTOR



(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	NC
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	BLON_OUT_C
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

## LCD POWER for ROSA



**CLOSED TO LVDS CONN LCD1**

**TPNPL**

5

1

2 USB\_PN0\_C

3 USB\_PP0\_C

4

6

1122 X02 Modify:  
stuff C4908 0.1uF from  
EMC Neo suggestion.

GP

ACES-C0N4-17-GP-U

**20.F1621.004**

**2nd = 20.F1561.004**

**3rd = 20.F1686.004**

621.004 from  
F.

61.004:3rd source  
from updated

TPNPL 5V

TPNPL

TPNE

R4904

5V\_S0

OR0402-PAD-2-GP

A00 1230

8

USB\_PN0 << >>

18

USB\_PP0 << >>

TR4901

TPNE

FILTER-4P-6-GP

**69.10103.041**

**2nd = 69.10084.071**

A00 1229

1122 X02 Modify:  
Swap TR4901 pin4,3 and pin2,1 each other  
base on Connie swap report.  
Change TR4901 CW choke to 69.10103.041  
and un-stuff R4911,R4912 from EMC Neo Suggestion.  
Change R4911,R4912 to 0603 from 0402.

**DN15ATIWhistler**

DN15ATI Whistle



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### LCD Connector

Size  
A3

ent Number

**QUEEN 15**

Date: Tuesday, January 04, 2011


Sheet 41

Rev	A00
-----	-----

108

( Blanking )

<Variant Name>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size  
A3

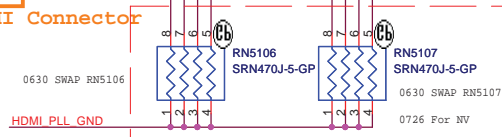
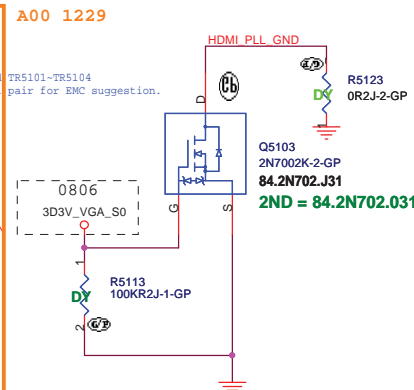
Document Number  
QUEEN 15

Date  
Tuesday, January 04, 2011

Rev  
A00

Sheet 50 of 108



**HDMI CONN**


## A00 1223 HDMI leakage

0629 Modify:  
Utilize Q5104 2N7002 instead of PCA9509 Level  
shifter base on Intel DG recommend on HDMI DDC

Title			
<b>HDMI Level Shifter/Connector</b>			
Size	Document Number	Rev	
A3	<b>QUEEN 15</b>	<b>A00</b>	
Date:	Tuesday, January 04, 2011	Sheet 51	of 108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 52 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**LVDS Switch**

Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

Date: Tuesday, January 04, 2011	Sheet 53 of 108
---------------------------------	-----------------

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 54 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

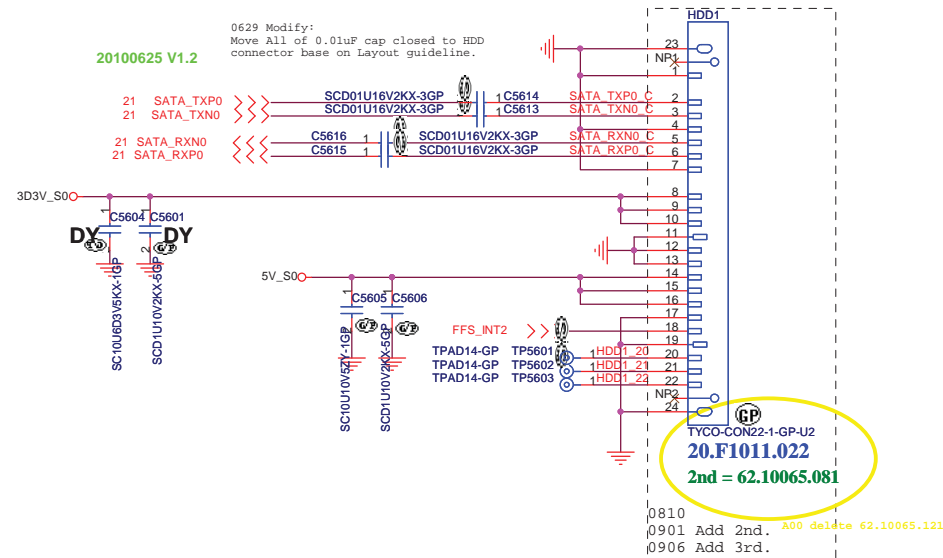
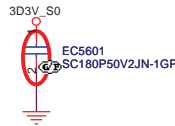
***ITP/Fan Connector***

Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

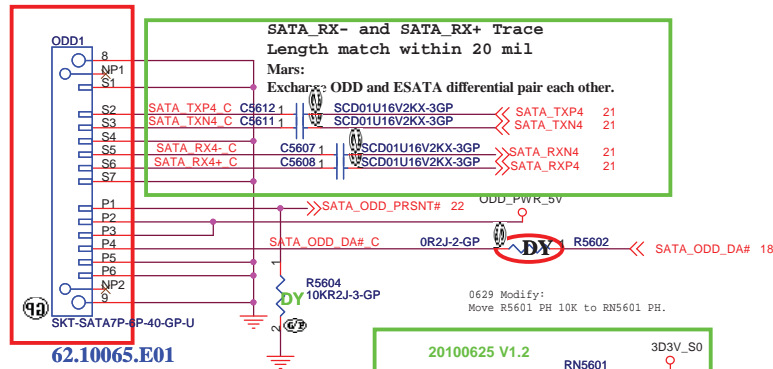
Date: Tuesday, January 04, 2011	Sheet 55 of 108
---------------------------------	-----------------

## SATA HDD Connector

1123 X02 Modify:  
stuff EC5601 180pF from RF  
fine tune result.

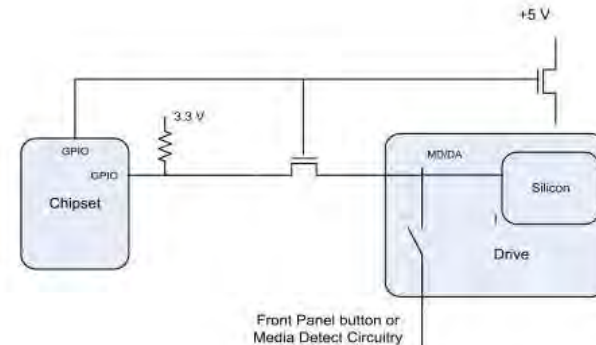
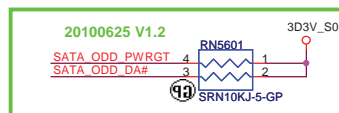


## ODD Connector

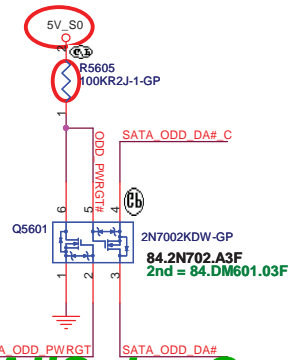


```
0614 Modify:
Change ODD1 connector part number to
22.10300.421 base on ME EMN and DXF.
0707 Modify:
Change ODD1 connector part number to
62.10065.E01 base on latest EMN and DXF.
```

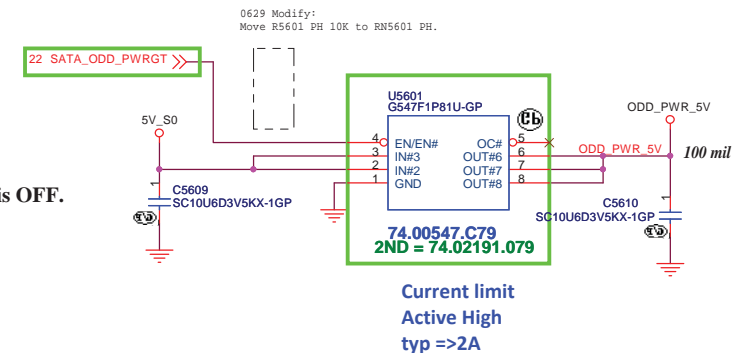
## SUPPORT ZERO SATA ODD



**When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON**



## SATA Zero Power ODD



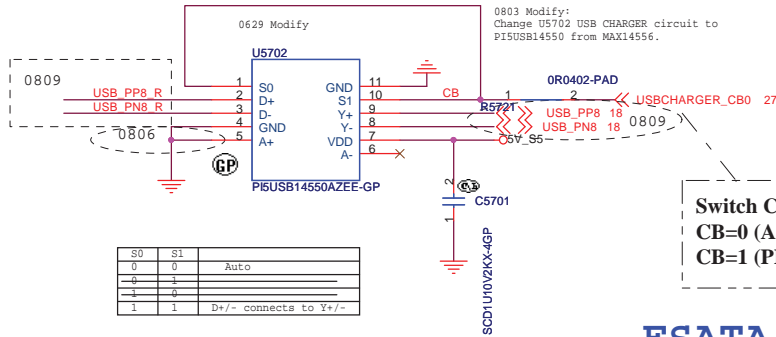
<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

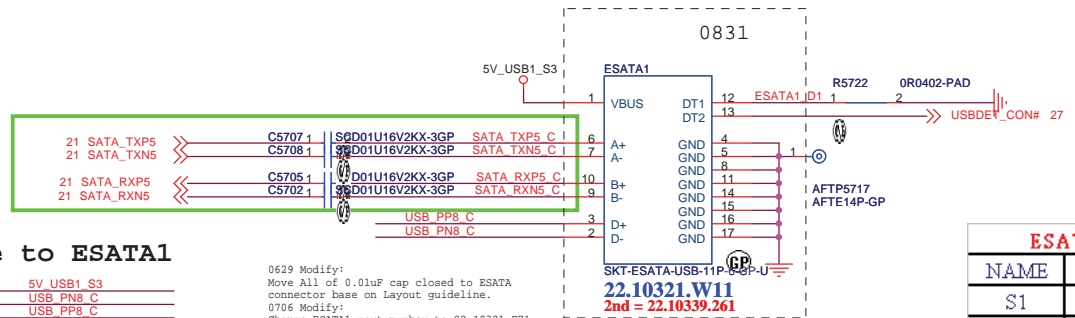
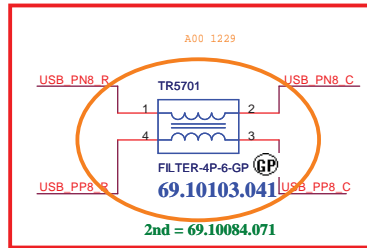


## USB CHARGER

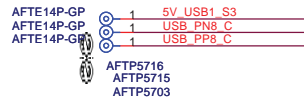


CB=0 (AM):auto detection charger identification active.  
CB=1 (PM):connect DP/DM to TDP/TDM.

## ESATA CONN



close to ESATA1



```

0629 Modify:
Move All of 0.01uF cap closed to ESATA
connector base on Layout guideline.
0706 Modify:
Change ESATA1 part number to 22.10321.F71
base on latest BOM and DFX.
0713 Modify:
Add USBDEF.CON# on ESATA1 pin1s for
USB temporary detect solution ESATA CONN
should be searched for detect type connector.
0719 Modify:
ME Double provide temporary foxconn ESATA conn
22.10290.141 for SST stage function test.

```

### E-SATA USB 2.0 Combo

**CE/H=-0.16/2.83mm with detect function**

ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

<Core Design>



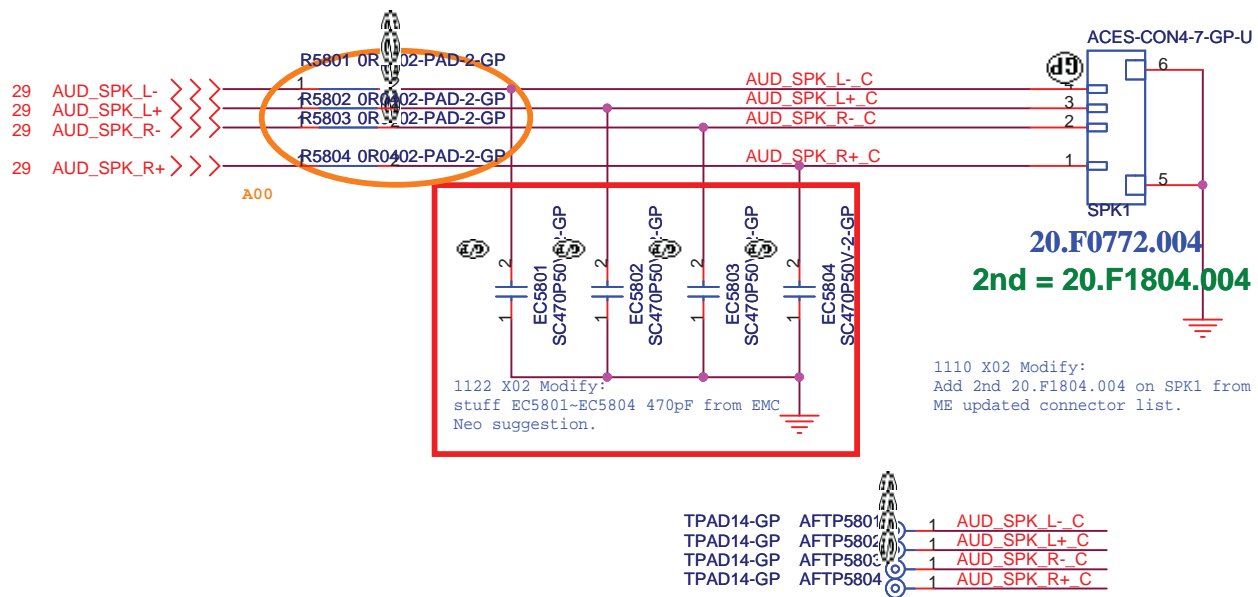
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>ESATA</b>
-------	--------------

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 57 of 108	

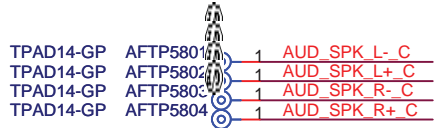
SSID = AUDIO

# Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0913 X01 Modify:  
Change SPK1 to 20.F0772.004 from  
20.F1647.004 from Double updated.  
0914 X01 Modify:  
Re-assign SPK1 pin define base on  
Roy updated excel file for 20.F0772.004



<Core Design>




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>SPEAKER CONN</b>		
Size A4	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date Tuesday, January 04, 2011	Sheet 58	of 108

( Blanking )

<Core Design>



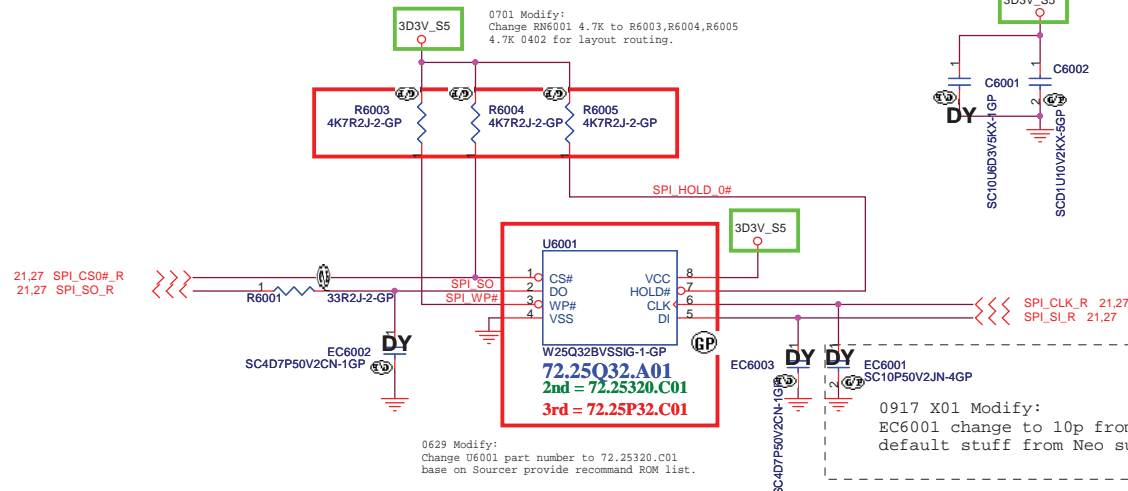
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 59 of	108

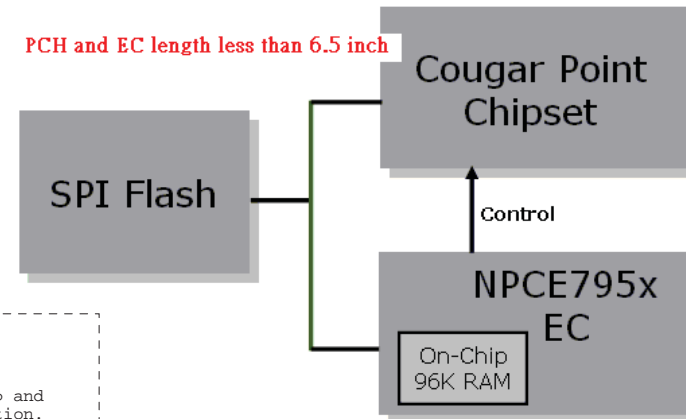
## SPI FLASH ROM (4M byte) for PCH



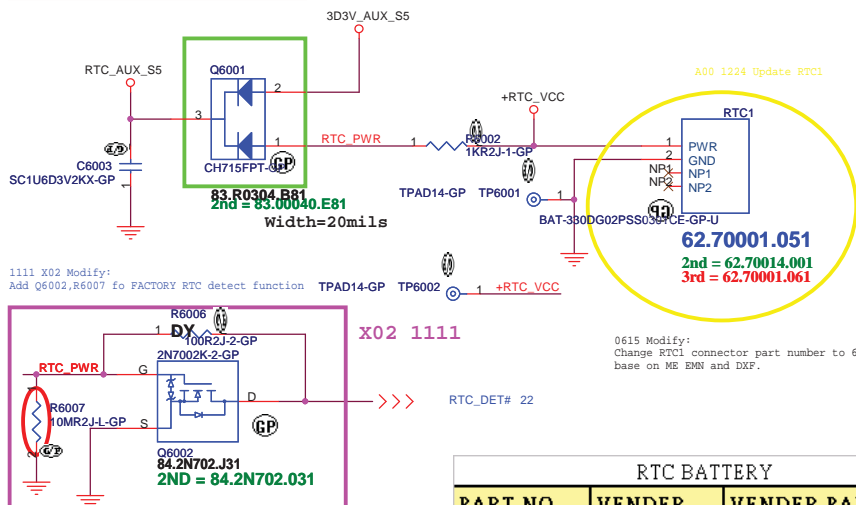
Pirority	Wistron P/N	Manufacturer	Vendor P/N
X02	1	72.25Q32.A01	WINBOND
	2	72.25320.C01	MXIC
X02	3	72.25P32.C01	Numonyx
			M25PX32-VMW6F

Notes:  
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

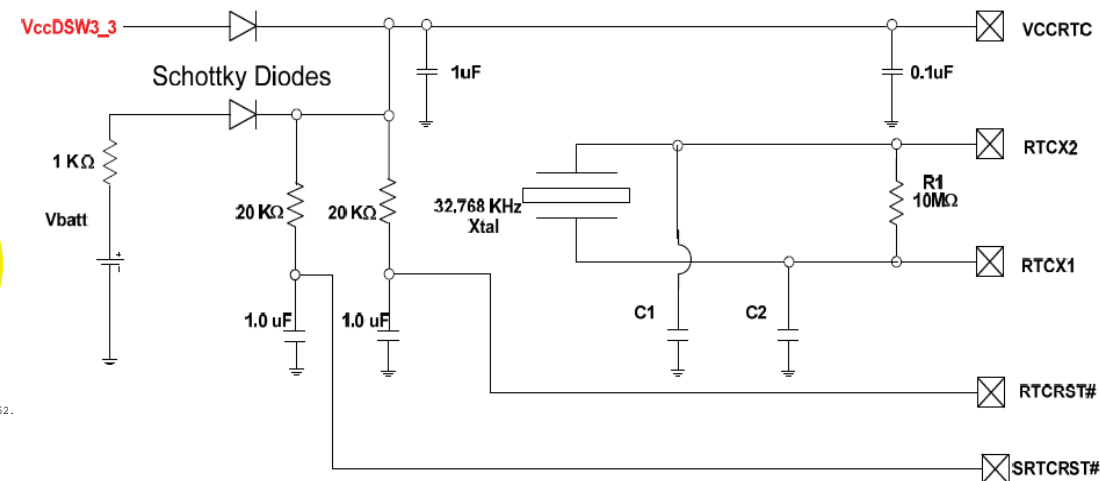
PCH and EC length less than 6.5 inch



## SSID = RBATT



RTC BATTERY		
PART NO	VENDER	VENDER PART NO.
23.20023.311	MITSUBISHI	CR2032 MITSUBISHI
23.20023.341	HENSHEN	CR-2032L/DBE
23.20068.001	KTS	BBBCR2032EV



VccRTC is now connected to VccDSW3\_3 through the Schottky diode instead of the 3.3V Sus well.

<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

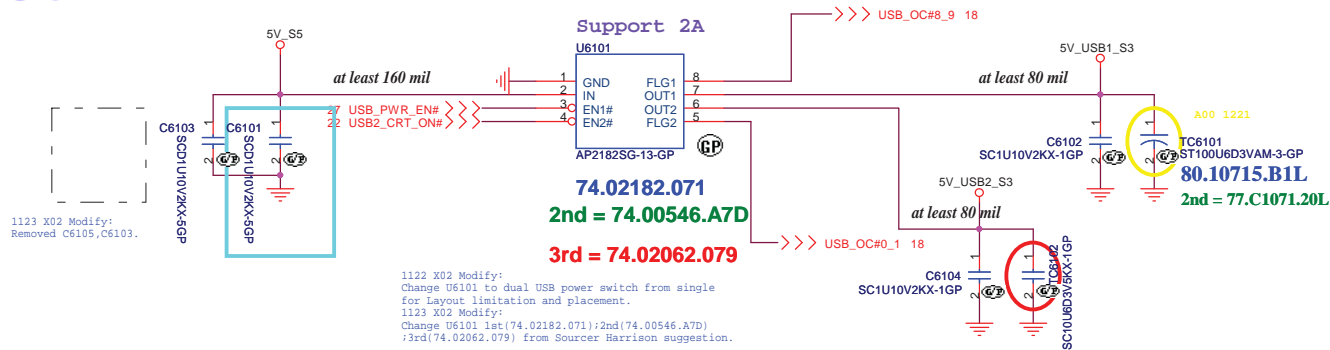
Title **Flash/RTC**

Size A3 Document Number **QUEEN 15** Rev **A00**

Date: Tuesday, January 04, 2011 Sheet 60 of 108

SSID = USB

## CRT Board and COMBO USB Power




<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB Power SW</b>			
Size	Document Number		Rev
	<b>QUEEN&amp;NIRVANA 15</b>		<b>A00</b>
Date: Tuesday, January 04, 2011		Sheet 61 of	108

( Blanking )

<Core Design>



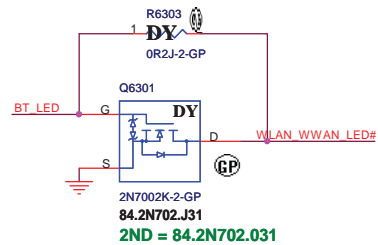
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

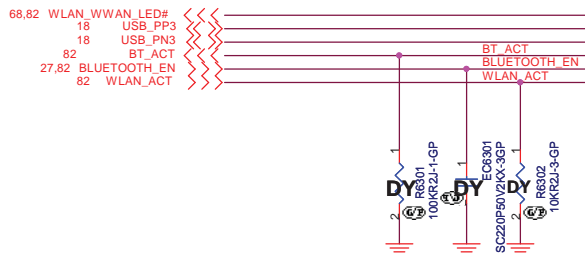
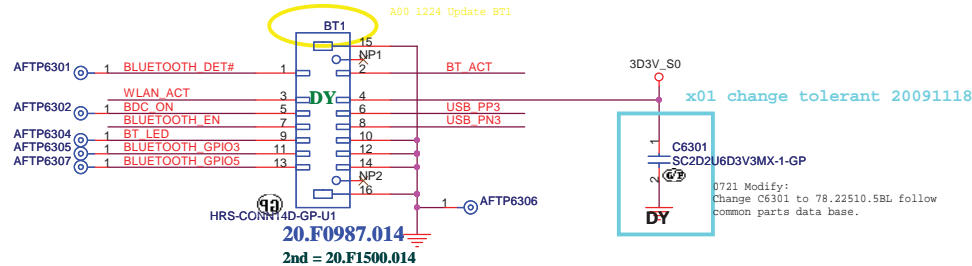
**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

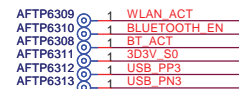
Date: Tuesday, January 04, 2011	Sheet 62 of 108
---------------------------------	-----------------



## Bluetooth Module conn.



0709 Modify:  
PM confirmed there is no stand-alone BT module,  
so DY BT1 connector, add BT enable signal  
and 5V\_S5 power option on WLAN connector pin 51.  
0712 Modify:  
Stuff BT relatek component to verify function.



<Core Design>



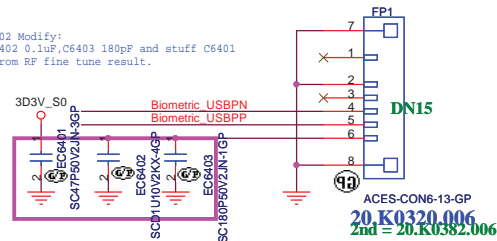
Title		Bluetooth	
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet	63 of 108



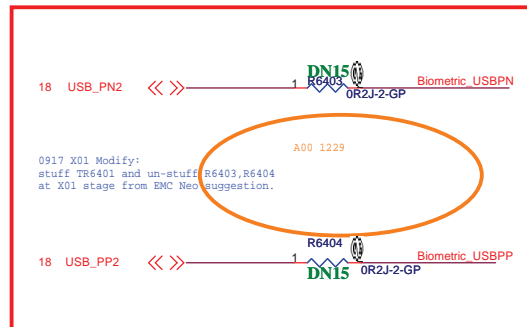
## Finger Printer Connector

0707 Modify:  
Add FP\_DET# signal on FP1 pin1.  
0715 Modify:  
Add FP\_DET# signal on FP1 pin1.  
0806 Swap pin.  
0810 Change to 4 pin.  
0827 Change to 6 pin.

1123 X02 Modify:  
Add C6402 0.1uF, C6403 180pF and stuff C6401  
47pF from RF fine tune result.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric USBPN
Pin5	Biometric USBPP
Pin6	3D3V_S0



AFTP42 1 3D3V\_S0  
AFTP43 1 Biometric USBPN  
AFTP44 1 Biometric USBPP


0615 Modify:  
Change FP1 connector part number to 20.K0320.004  
base on ME EMN and DXF.  
0630 Modify:  
Change FP1 connector part number to 20.K0320.006  
base on ME EMN and DXF.  
0707 Modify:  
Reassign Finger print pin define base on EXCEL FILE.  
0713 Modify:  
Reassign Finger print pin define base on EXCEL FILE.  
Removed FP\_DET# on FP1.

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size A3	Document Number QUEEN 15		Rev A00
Date: Tuesday, January 04, 2011	Sheet	64	of 108

(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**RESERVED**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 65 of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Tuesday, January 04, 2011	Sheet 66 of 108
---------------------------------	-----------------

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

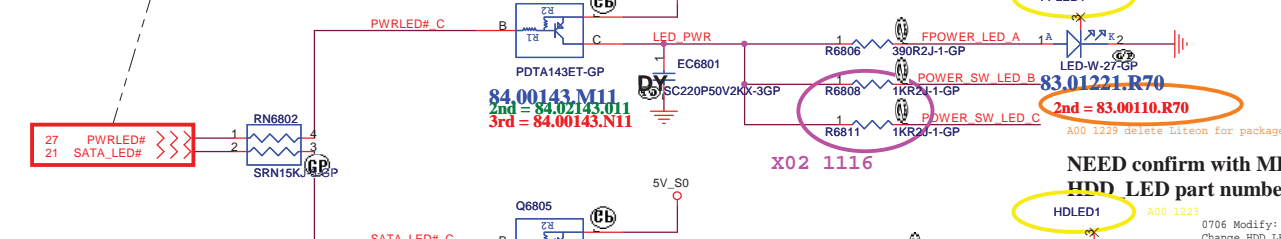
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Tuesday, January 04, 2011	Sheet 67 of 108
---------------------------------	-----------------

SSID = User.Interface

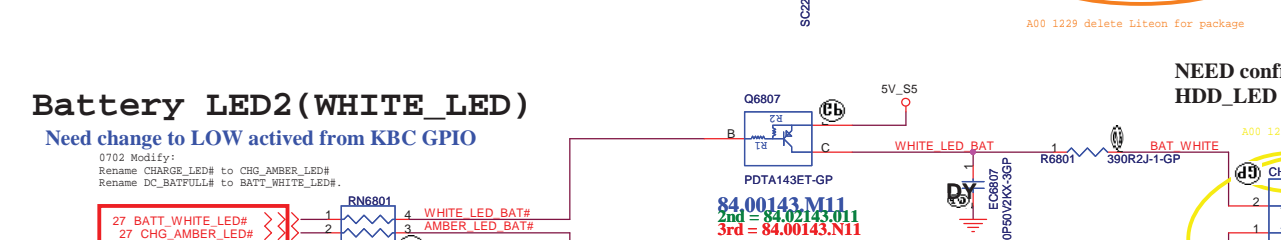
## FRONT POWER LED

Need change to LOW acted from KBC GPIO



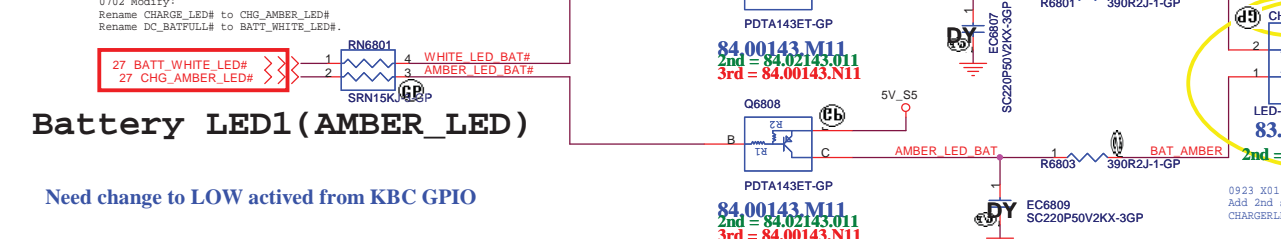
## SATA HDD LED(White)

Need change to LOW acted from KBC GPIO



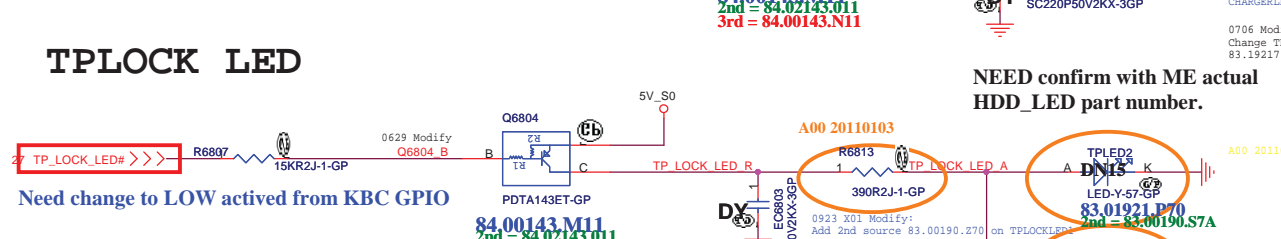
## Battery LED2(WHITE\_LED)

Need change to LOW acted from KBC GPIO



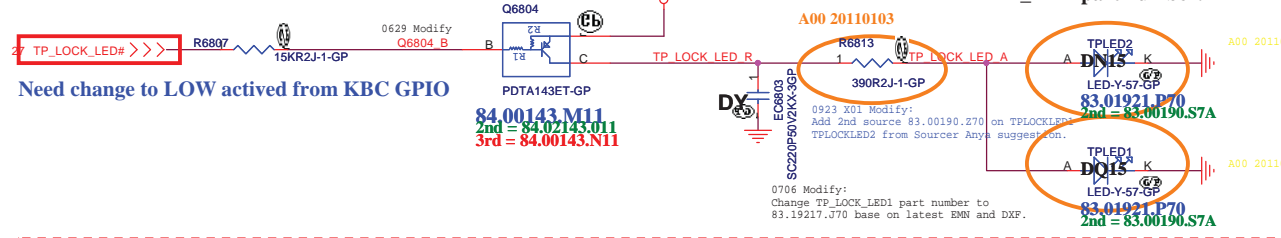
## Battery LED1(AMBER\_LED)

Need change to LOW acted from KBC GPIO

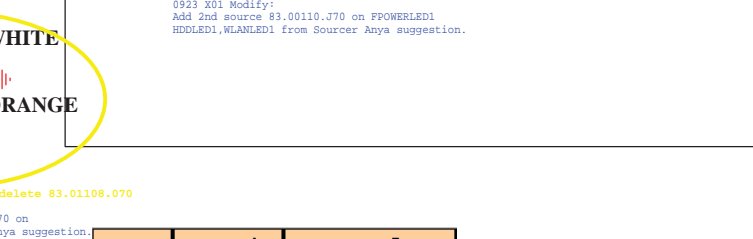
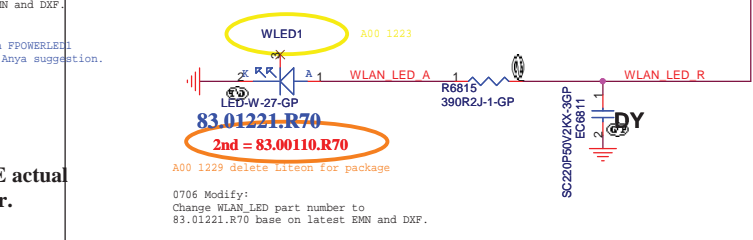
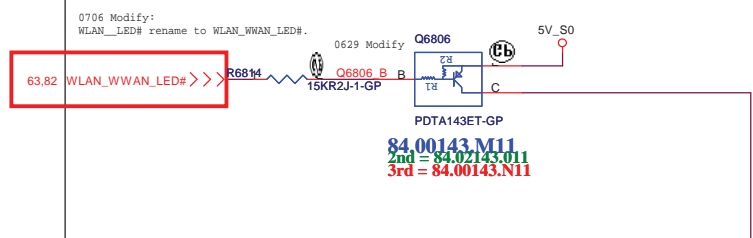


## TPLOCK LED

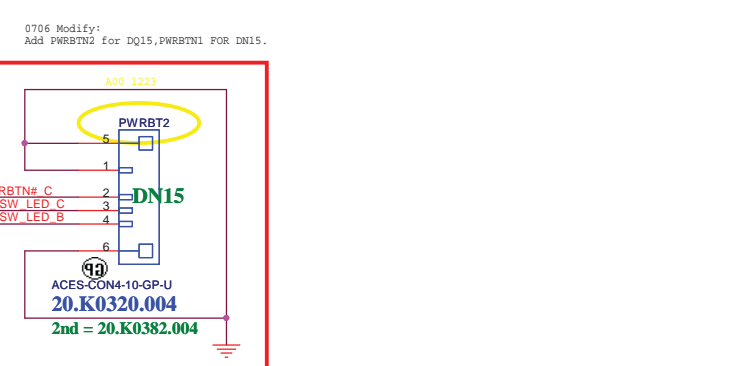
Need change to LOW acted from KBC GPIO



## WLAN\_LED



SKEW	ITEM1	ITEM2
DQ15	PWRBTN1	TP_LOCK_LED1
DN15	PWRBTN2	TP_LOCK_LED2



**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **LED Bard/Power Button**

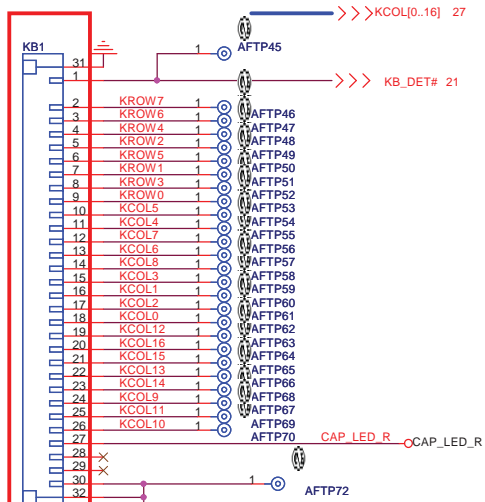
Size A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet 68 of 108

SSID = KBC

## Internal Keyboard Connector

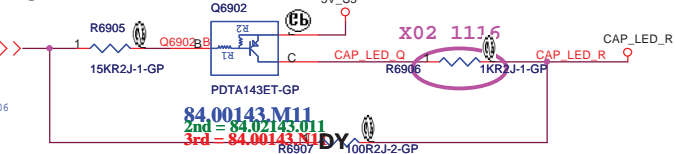
0630 Modify:  
Change KB1 part number to 20.K0565.030  
base on ME updated EMN and DMF.



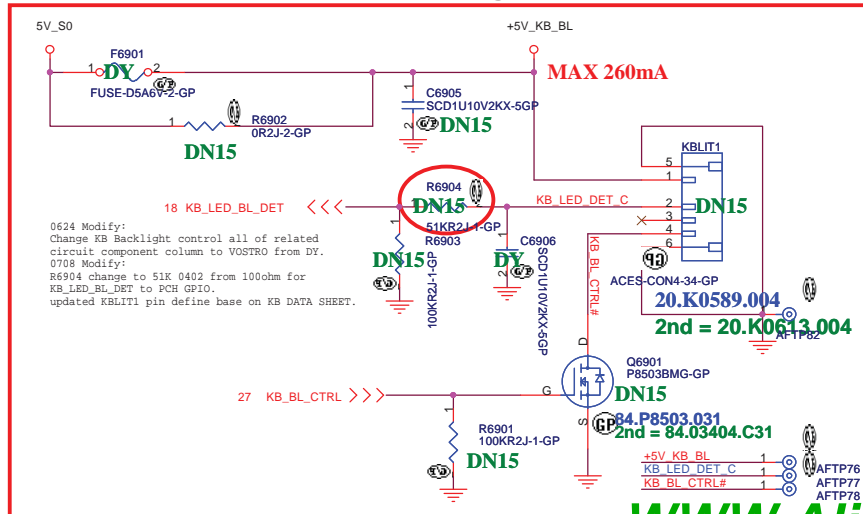
MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

## CAP LED CONTROL

High Active from KBC GPIO.

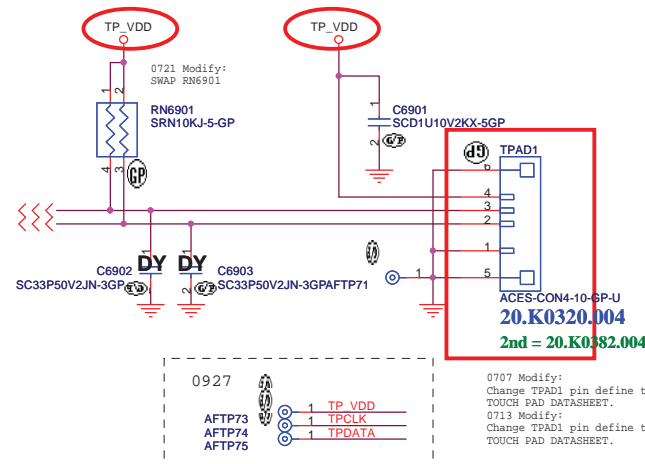


## KB Backlight Connector



SSID = Touch.Pad

## TouchPad Connector

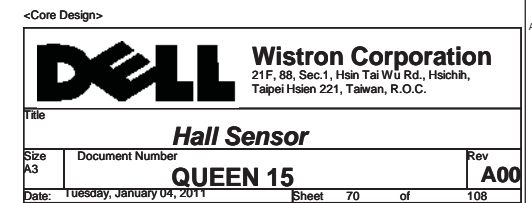


MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

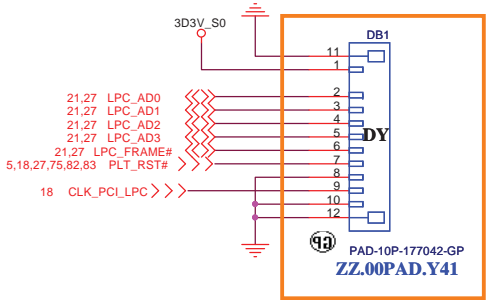
SKEW	OPTION1	OPTION2	PIN	Feature	REMARK
DQ13	C12S		30		S is mean small
DN13	C12S	C12SB	30/25	Backlight	SB is mean small with backlight
DN15	C12S	C12SB	30/25	Backlight	
DQ15	C12SN		30	KB_DET#,CAP LED	SN is mean small with numpad

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

0901 X01 Modify:  
Change KBLIT1 to 20.K0320.004 from 20.K0218.004 base on ME updated X01 DXF&EMN.  
Re-assign KBLIT1 pin define sync with DQ15\_NV.  
0914 X01 Modify:  
Add 2nd source 20.K0382.004 on KBLIT1 base on updated connector list.  
0923 X01 Modify:  
Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.








A00 1229 DB1 change to ZZ.00PAD.Y41(solder kmask type)  
and keep un-stuffat X-Build stage

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 72 of 108	

( Blanking )

<Core Design>

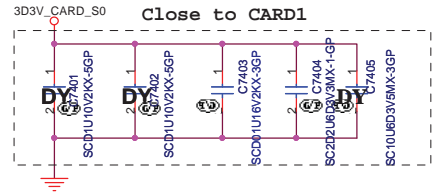
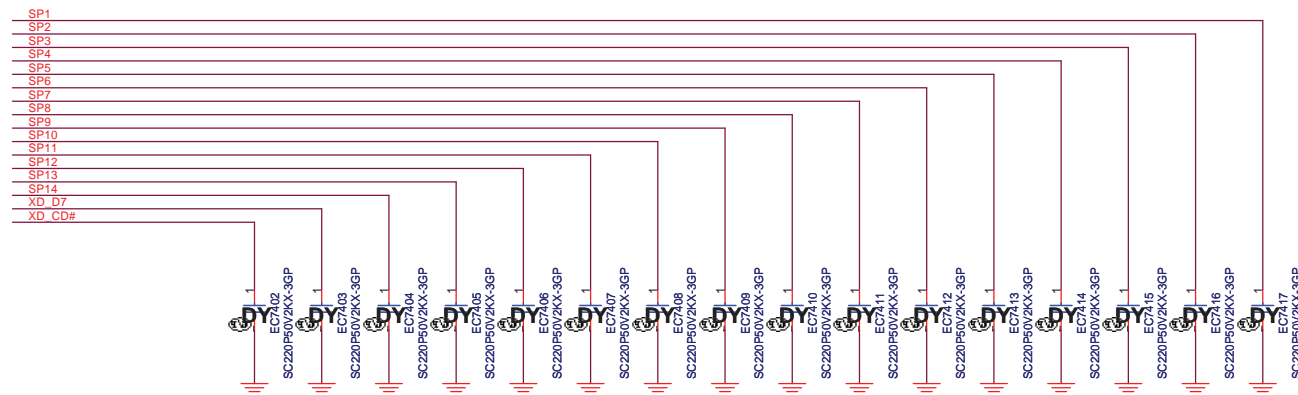



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

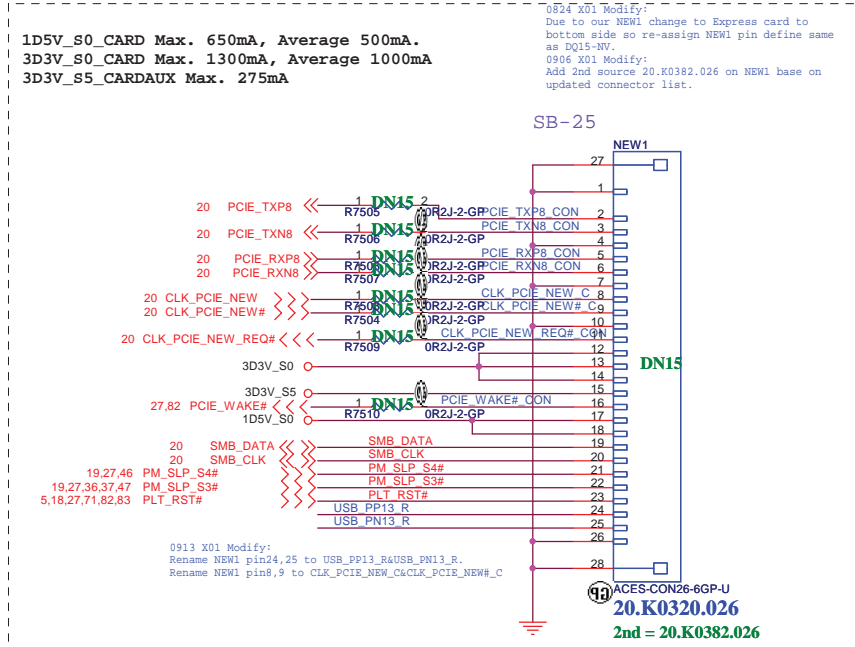
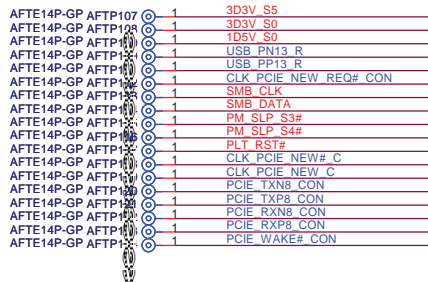
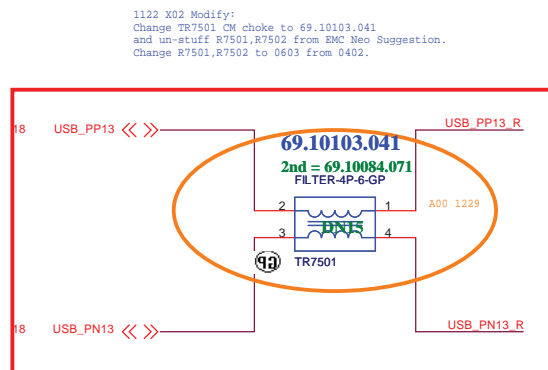
Title

**Reserved**

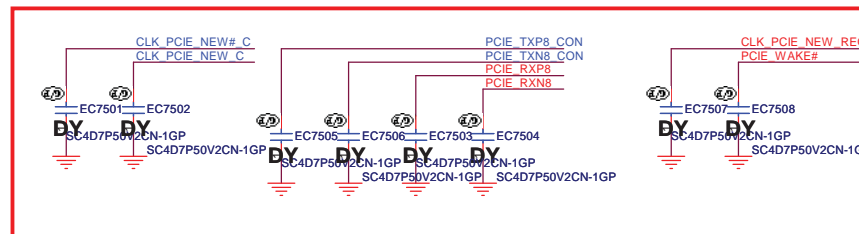
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 73 of	108

[illegible]

<Core Design>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>SD/XD/MS/MMC Card CONN</b>			
Size A3	Document Number	Rev	
	<b>QUEEN 15</b>	<b>A00</b>	
Date:	Tuesday, January 04, 2011	Sheet	74 of 108



#### For EMI




0913 X01 Modify:  
Add R7503,R7504 and reserved EC7501,EC7502 on CLK\_PCIE\_NEW & CLK\_PCIE\_NEW# for EMC suggestion.  
0921 X01 Modify:  
Add R7505-R7508 0ohm and reserved EC7503-EC7506 on PCIE\_TXN8&PCIE\_TXP8 signal base on EMC Lance suggestion.  
Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK\_PCIE\_NEW\_REQ#&PCIE\_WAKE# signal base on EMC Lance suggestion.

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Express Card</b>			
Size A3	Document Number	Rev	
	<b>QUEEN 15</b>		
Date: Tuesday, January 04, 2011	Sheet 75	of	108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Tuesday, January 04, 2011	Sheet 76 of 108
---------------------------------	-----------------

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 77 of 108	



( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

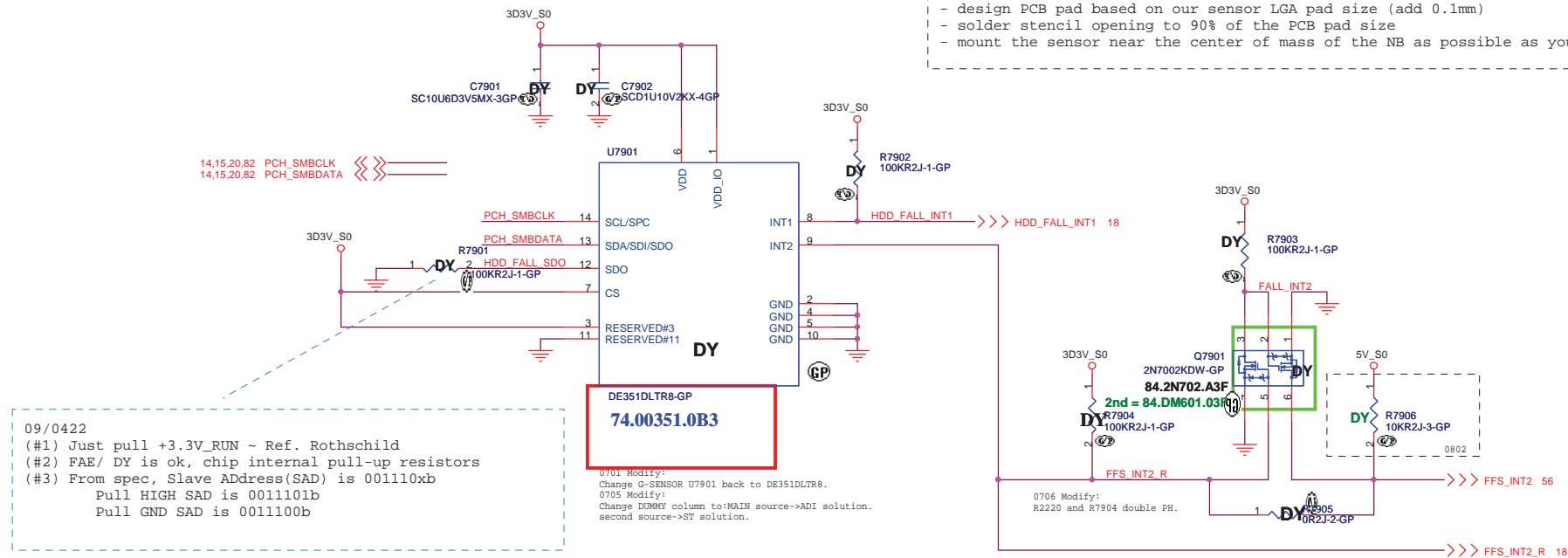
**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 78 of	108

## Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

### <Core Design>

DELL

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### ***Free Fall Sensor***

Size	A3
------	----

Document Number
-----------------

**QUEEN 15**

Rev

A00


Date: Tuesday, January 04, 2011

Sheet 7

9 of 108

( Blanking )

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Tuesday, January 04, 2011	Sheet 80 of 108
---------------------------------	-----------------

( Blanking )

<Core Design>

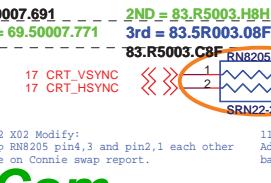
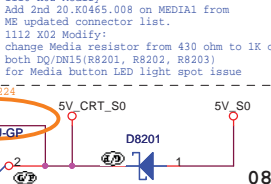
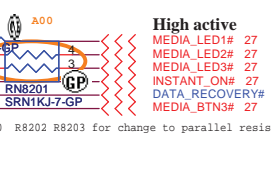
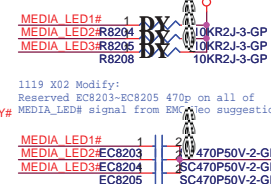
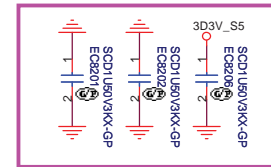
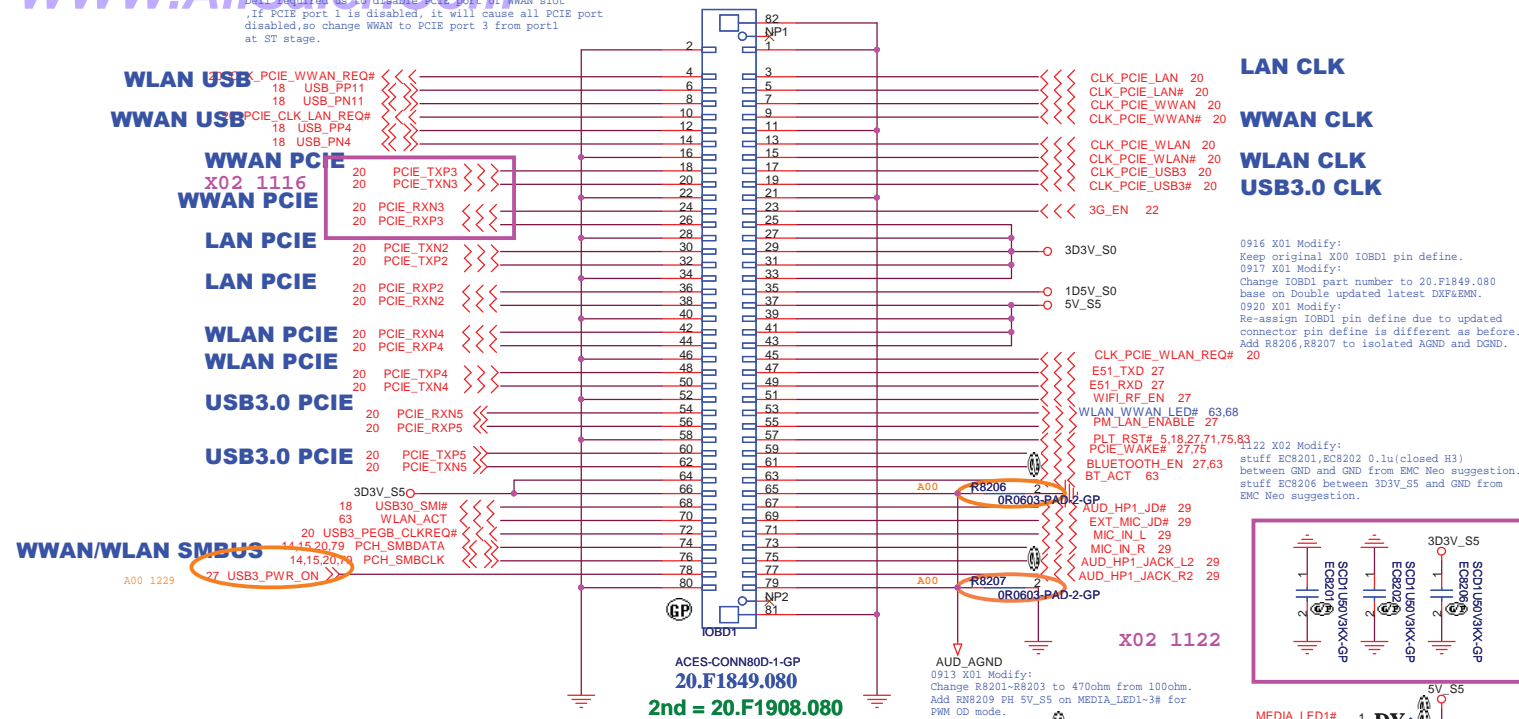


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 81 of	108

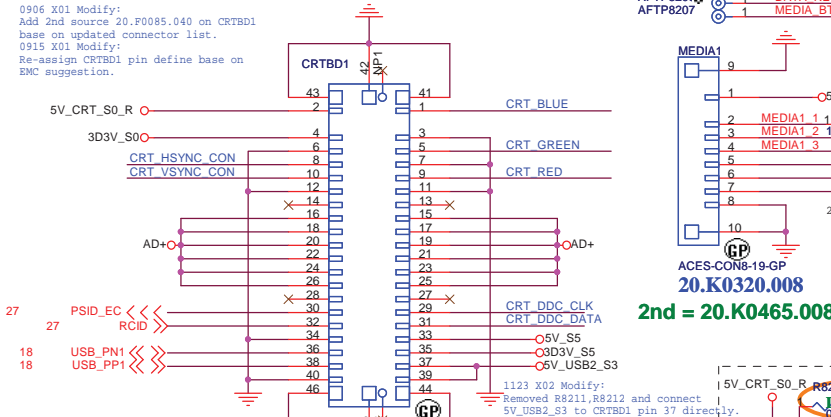


SIGNAL	PIN	PIN	SIGNAL
GND	80	79	GND
CLK_PCIE_WWAN_REQ#	78	77	CLK_PCIE_LAN
USB_PP11	76	75	CLK_PCIE_LAN#
USB_PN11	74	73	CLK_PCIE_WWAN
PCIE_CLK_LAN_REQ#	72	71	CLK_PCIE_WWAN#
USB_PP4	70	69	GND
USB_PN4	68	67	CLK_PCIE_WLAN
GND	66	65	CLK_PCIE_WLAN#
PCIE_TXP1	64	63	CLK_PCIE_USB3
PCIE_TXN1	62	61	CLK_PCIE_USB3#
GND	60	59	GND
PCIE_RXN1	58	57	3G_EN
PCIE_RXP1	56	55	3D3V_S0
GND	54	53	3D3V_S0
PCIE_TXN2	52	51	3D3V_S0
PCIE_TXP2	50	49	3D3V_S0
GND	48	47	3D3V_S0
PCIE_RXP2	46	45	1D5V_S0
PCIE_RXN2	44	43	5V_S5
GND	42	41	5V_S5
PCIE_RXN4	40	39	5V_S5
PCIE_RXP4	38	37	5V_S5
GND	36	35	CLK_PCIE_WLAN_REQ#
PCIE_TXP4	34	33	E51_TXD
PCIE_TXN4	32	31	E51_RXD
GND	30	29	WIFI_RF_EN
IOBD1_28	28	27	WLAN_WWAN_LED#
IOBD1_26	26	25	PM_LAN_ENABLE
GND	24	23	PLT_RST#
IOBD1_22	22	21	PCIE_WAKE#
IOBD1_20	20	19	BLUETOOTH_EN
3D3V_S5	18	17	BT_ACT
3D3V_S5	16	15	GND
IOBD1_14	14	13	AUD_HP1_JD#
WLAN_ACT	12	11	EXT_MIC_JD#
USB3_PEGB_CLKREQ#	10	9	MIC_IN_L
PCH_SMBDATA	8	7	MIC_IN_R
PCH_SMBCLK	6	5	AUD_HP1_JACK_L2
USB3_PWR_ON	4	3	AUD_HP1_JACK_R2
GND	2	1	GND

USB3.0 PCIE  
USB3.0 PCIE

SIGNAL	PIN	PIN	SIGNAL
5V_CRT_S0_R	2	1	CRT_BLUE_R
3D3V_S0	4	3	GND
GND	6	5	CRT_GREEN_F
CRT_HSYNC_CON	8	7	GND
CRT_VSYNC_CON	10	9	CRT_RED_R
GND	12	11	GND
NC	14	13	NC
AD+	16	15	AD+
AD+	18	17	AD+
AD+	20	19	AD+
AD+	22	21	AD+
AD+	24	23	AD+
AD+	26	25	AD+
NC	28	27	NC
PSID_EC	30	29	DDCCLK
RCID	32	31	DDCDATA
GND	34	33	5V_S5
USB_PN1	36	35	3D3V_S5
USB_PP1	38	37	5V_USB1_S3
GND	40	39	5V_USB1_S3

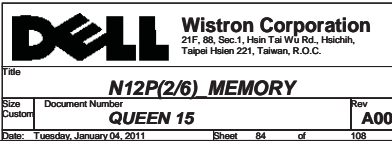
## CRT Board Connector



base on Connie swap

<Core Design>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>IO Board Connector</i></b>			
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A0</b>	
Date:	Tuesday, January 04, 2011	Sheet	62 of 108





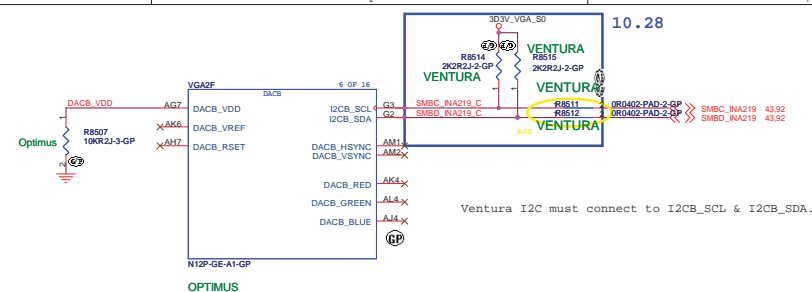
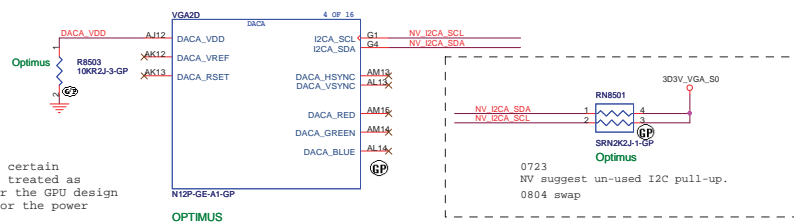
If a DAC interface is not required, it should be disabled by:

1. Adding a pull-down to the DACx VDD with a 10 kilohm resistor to GND.
2. All other DAC I/O pins can be left floating.

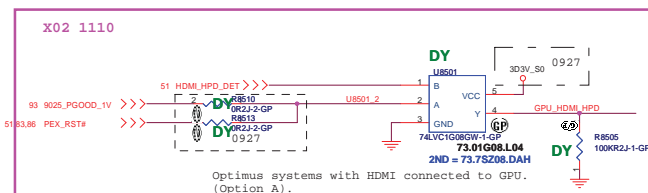
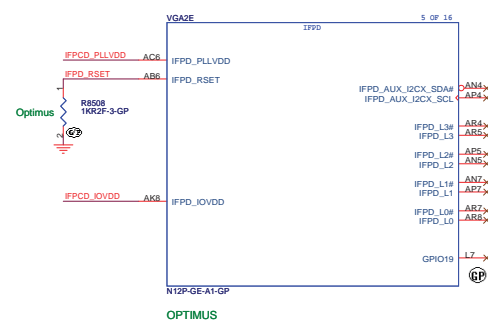
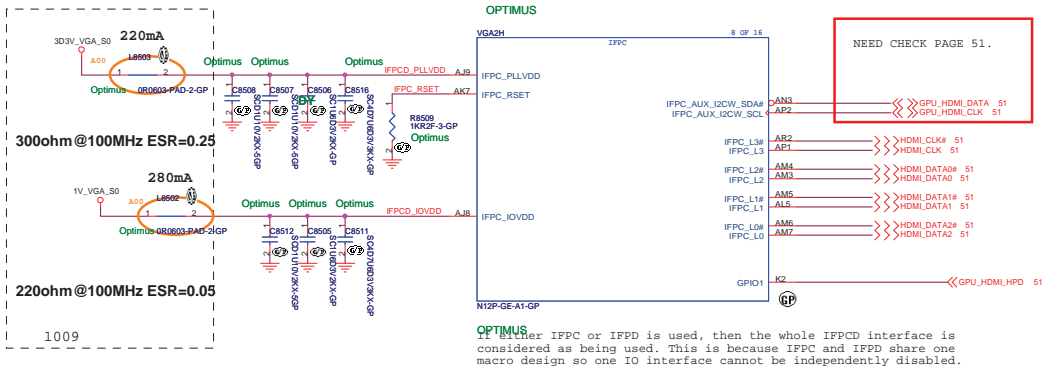
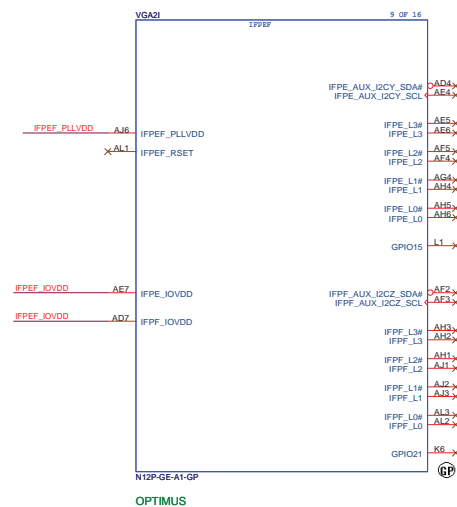
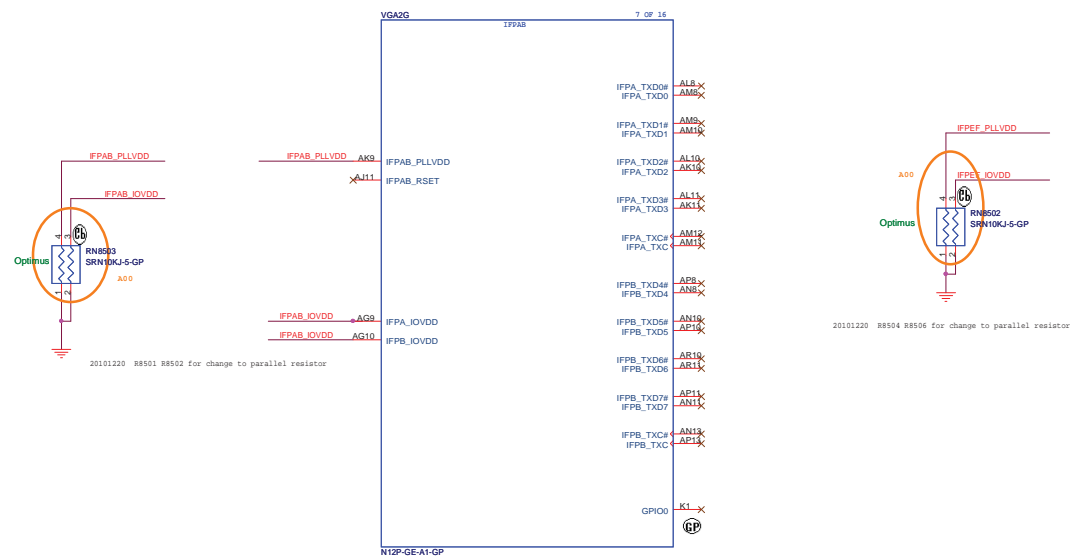
In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied to the signal or the power supply block.

The following guidelines only apply to a fully unused IFP macro:

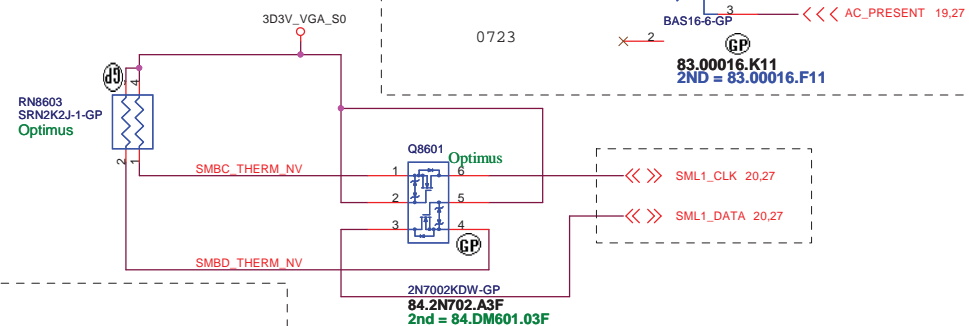
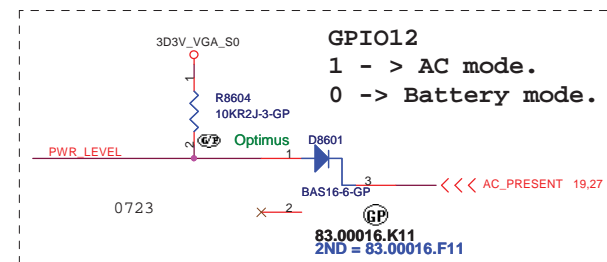
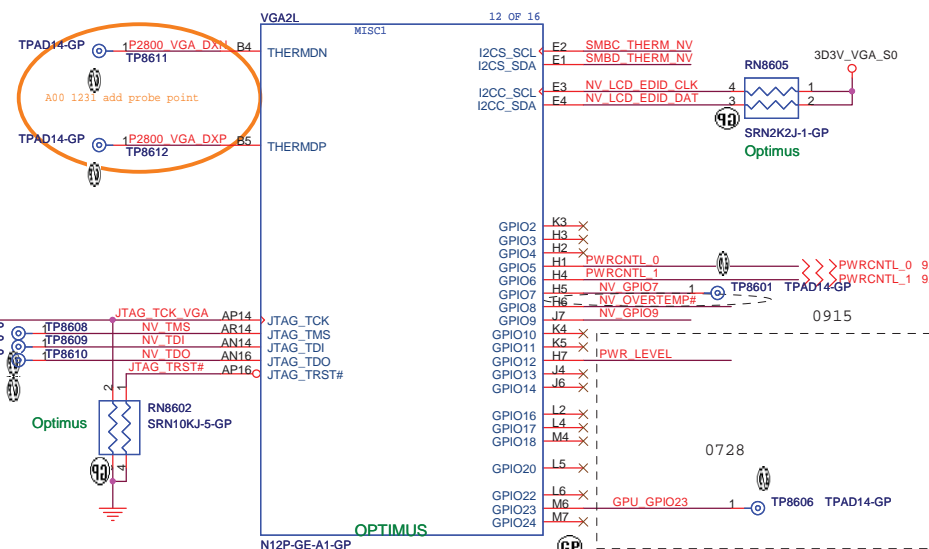
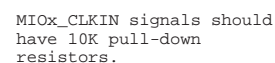
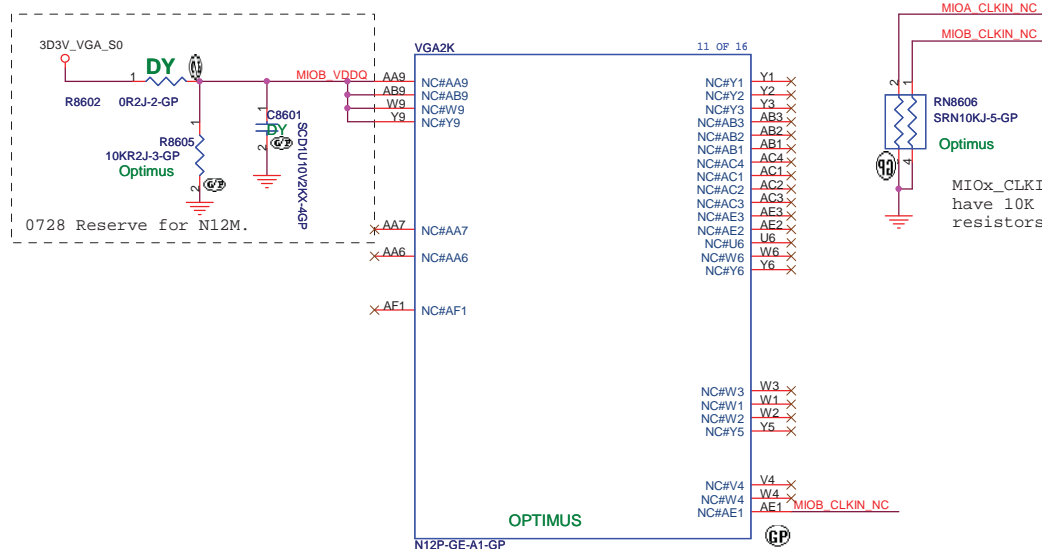
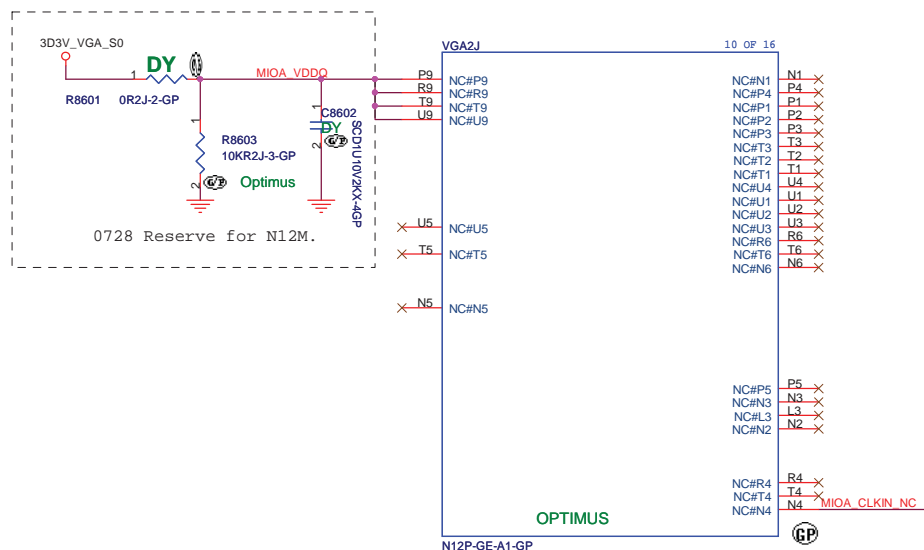
1. Pull down IFPxy\_IOVDD with 10 kilohm resistor.
2. Pull down IFPxy\_PLLVDD with 10 kilohm resistor.
3. The other IO pins can be NC; this includes unused data lines.



Ventura I2C must connect to I2CB SCL & I2CB SDA

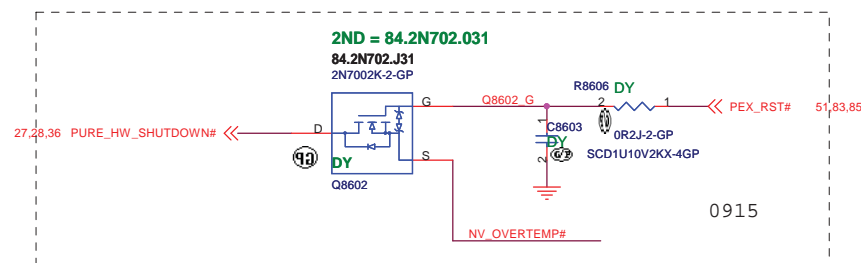






MIOA/B Support

Package	MIOA	MIOB
GB1-192	15-bit, available	TBD
GB2-128	Not available	Not available

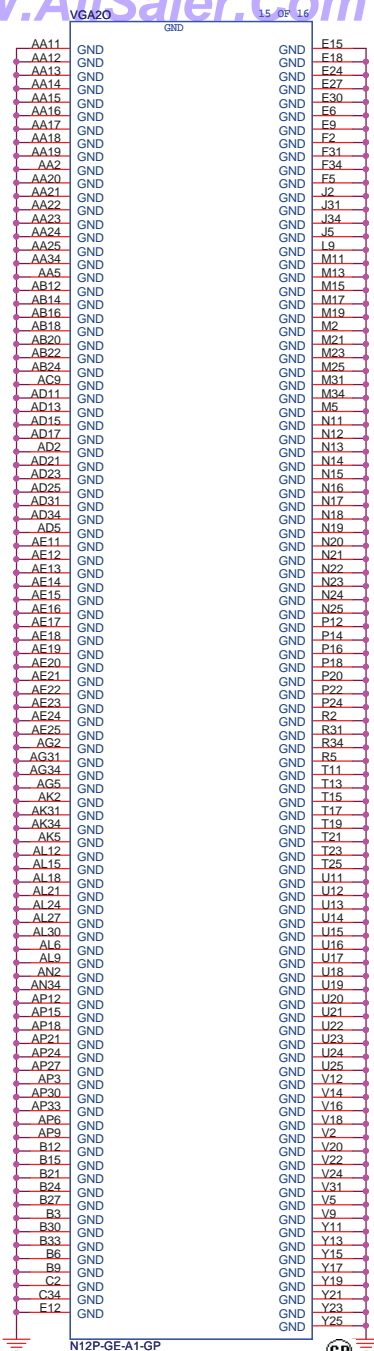


<Variant Name>

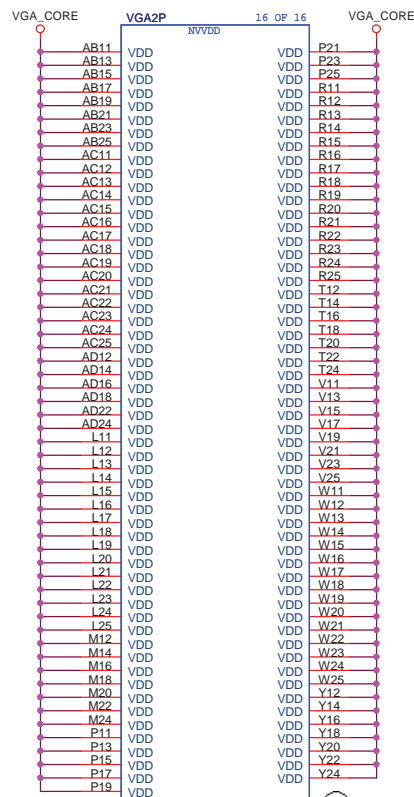


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

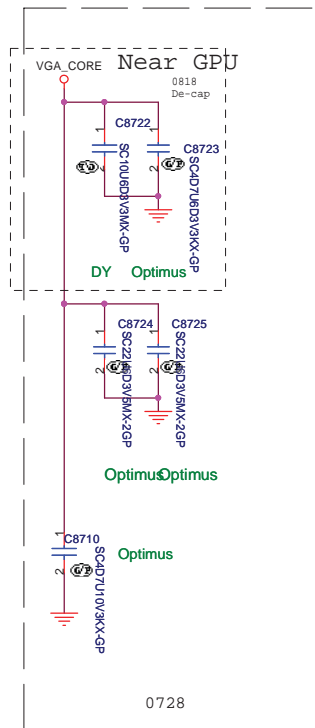
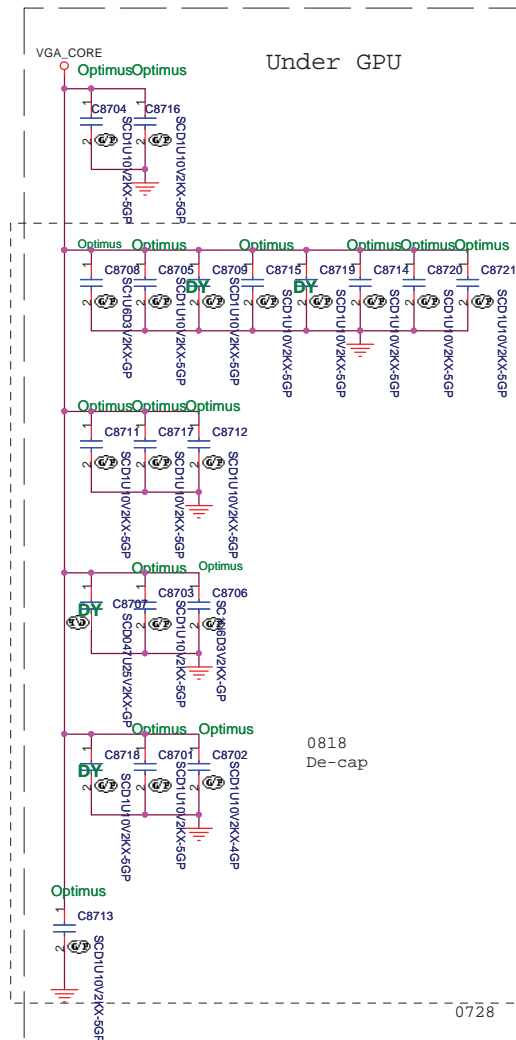
Title			
<b>N12P(5/6) MIO/ GPIO</b>			
Size A3	Document Number		Rev
	<b>QUEEN 15</b>		<b>A00</b>
Date:	Tuesday, January 04, 2011	Sheet 86 of	108



OPTIMUS



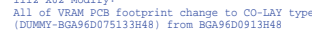
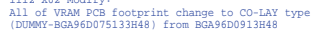
OPTIMUS



<Variant Name>

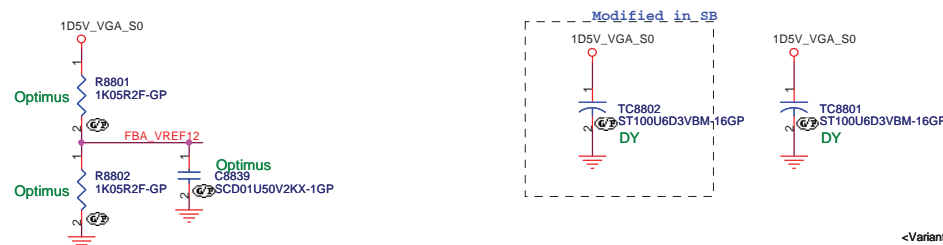
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

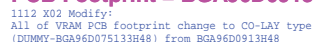
Title			<b>N12P(6/6) POWER</b>	
Size	Document Number	Rev		
A3	<b>QUEEN 15</b>	<b>A00</b>		
Date:	Tuesday, January 04, 2011	Sheet	87	of 108



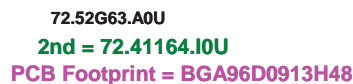
&lt;Variant Name&gt;

GB1-128 Mode C	GB2-128	DRAM Function	
Single Rank	Mode E	0-31	32-63
CM025	CM00	ODT	
CM026	CM01	CS1†	
CM02	CM02	CS0†	
CM027	CM03	CKE	
CM010	CM04	A3	A11
CM028	CM05	A6	A7
CM147	CM06	A3	BA1
CM029	CM07	A0	A12
CM03	CM08	A8	A8
CM022	CM09	A12	A0
CM021	CM10	A1	A2
CM024	CM011	RA5*	RA4*
CM018	CM12	A13	A14
CM023	CM13	BA3	A3
CM029	CM14	A14	A13
CM025	CM15	CA5*	CA5*
CM027	CM16	QWE	QWE
CM015	CM17	CS1*	
CM018	CM18	CS0*	
CM016	CM19	ODT	
CM028	CM20	RST	RST
CM026	CM21	A7	A6
CM017	CM22	A4	A5
CM06	CM23	A11	A9
CM02	CM24	A2	A1
CM021	CM25	A10	WE1*
CM02	CM26	A5	A4
CM013	CM27	BA2	A15
CM019	CM28	WE*	A10
CM02	CM29	BA0	BA0
CM030	CM30	A15	BA2





**WWW.AliSaler.Com**



1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMY-BGA96D075133H48) from BGA96D0913H48



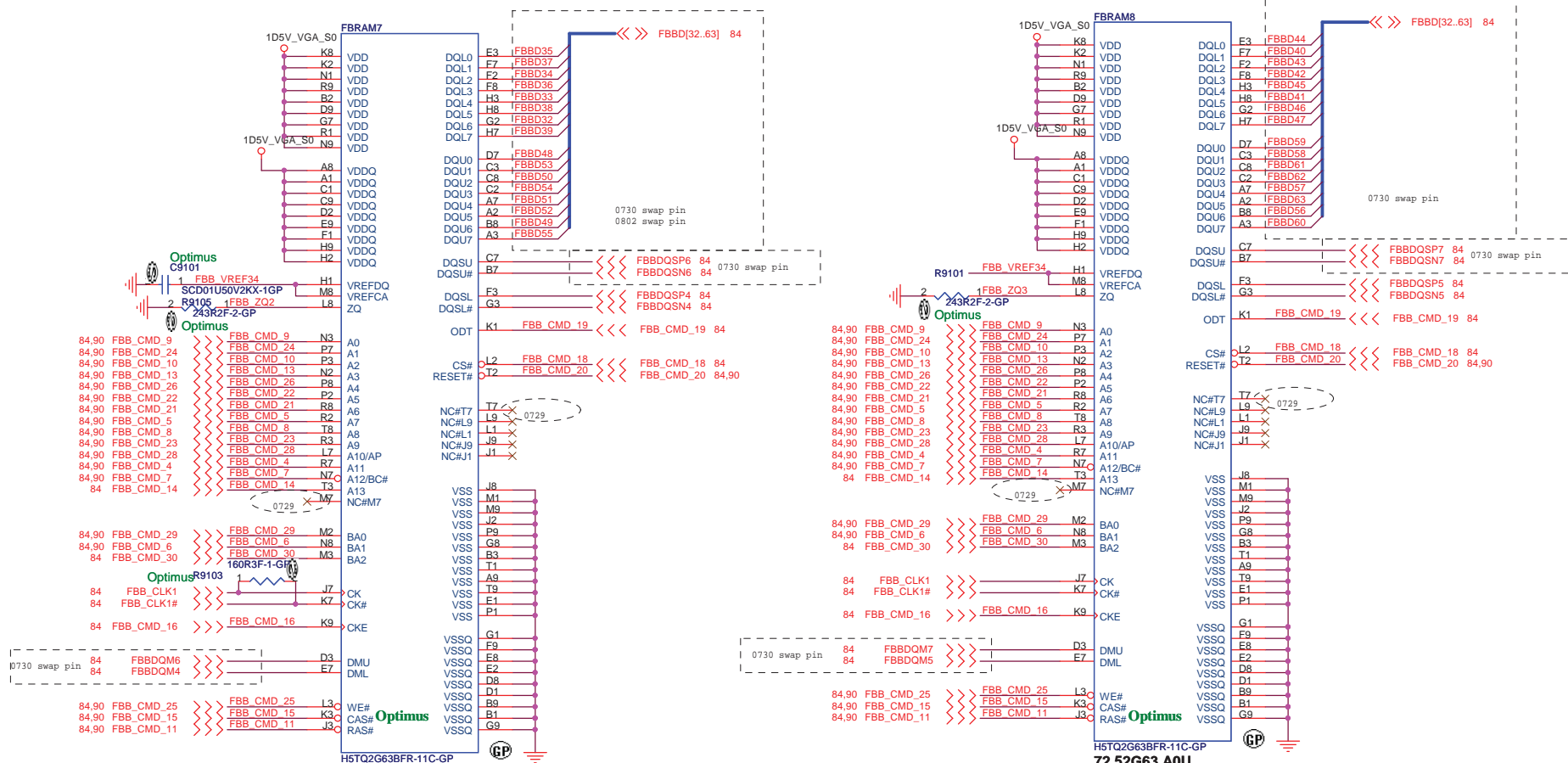
1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMY-BGA96D075133H48) from BGA96D0913H48

**VRAM(3/4)**

**QUEEN 15**

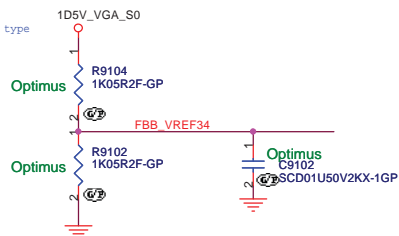
Sheet 90 of 108

# Frame Buffer Partition B Upper 32 bits.



**72.52G63.A0U**  
**2nd = 72.41164.I0U**  
**PCB Footprint = BGA96D0913H48**

1112 X02 Modify:  
 All of VRAM PCB footprint change to CO-LAY type  
 (DUMMT-BGA96D075133H48) from BGA96D0913H48



**2nd = 72.41164.I0U**  
**PCB Footprint = BGA96D0913H48**

1112 X02 Modify:  
 All of VRAM PCB footprint change to CO-LAY type  
 (DUMMT-BGA96D075133H48) from BGA96D0913H48

<Variant Name>

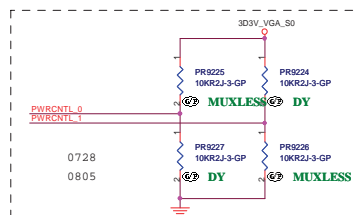
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>VRAM(4/4)</b>		
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 91	of 108



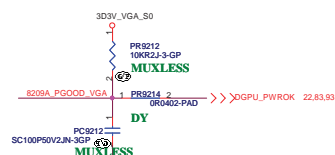
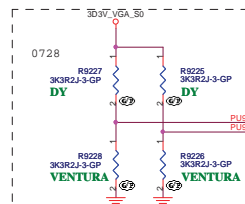
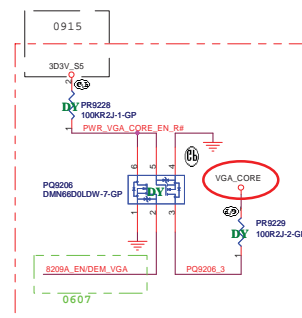


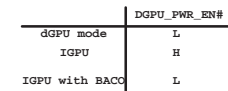
P-State	PWRCTRL_1 (GPIO6)	PWRCTRL_0 (GPIO5)	VGA_CORE_PWR
P0 (Cold)	L	L	0.975V
P0 (Hot)	L	H	0.954V (default boot up)
ES	H	L	0.876V
P8 & P12	H	H	0.853V

0923  
Update value of PR9210, PR9209 and PR9213  
for N12P.

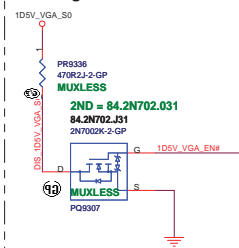


```
Frequency setting
470K  -->165KHz
200K  -->323KHz
100K  -->500KHz
```





1D5V\_VGA\_S0



```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay
after VGA_Core
```


0714 Modify:  
Change LDO to Max 4A.



Size A2	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 02 of 108	




(Blanking)

<Variant Name>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>LVDS Switch</b>			
Size A3	Document Number <b>QUEEN 15</b>		Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet	94	of 108

(Blanking)

<Variant Name>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Switch

Size  
A3

Document Number  
**QUEEN 15**

Rev  
**A00**


Date: Tuesday, January 04, 2011

Sheet 95 of 108

SSID = SDIO

( Blanking )

<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**TOUCH PANEL**

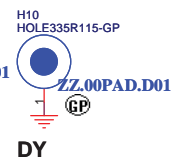
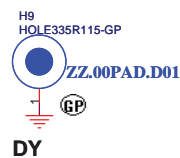
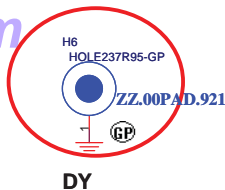
Size  
A3

Document Number  
**QUEEN 15**

Rev  
**A00**

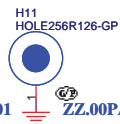
Date: Tuesday, January 04, 2011

Sheet 96 of 108

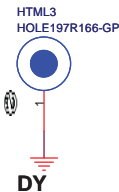
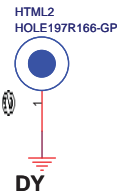
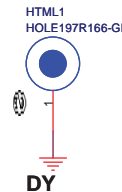


Check test point

0624 Modify:  
Removed AFTP1,AFTP7-AFTP13.

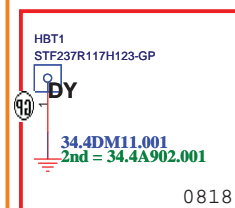
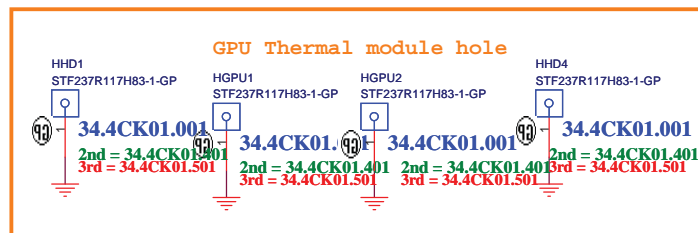
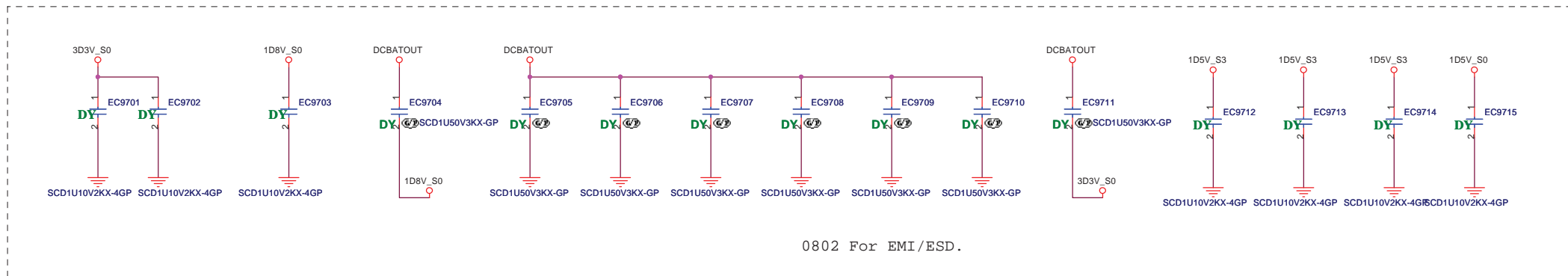
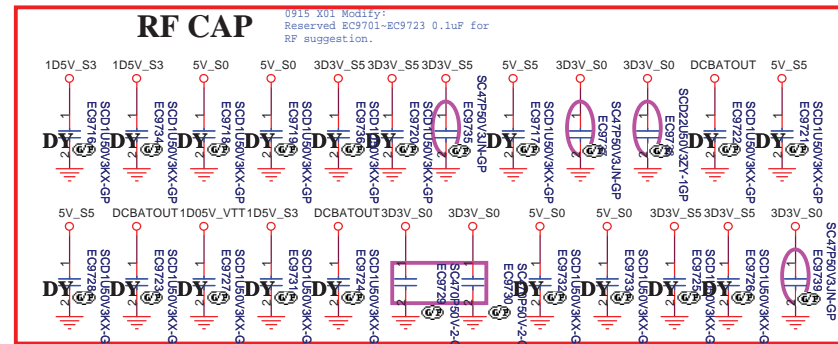
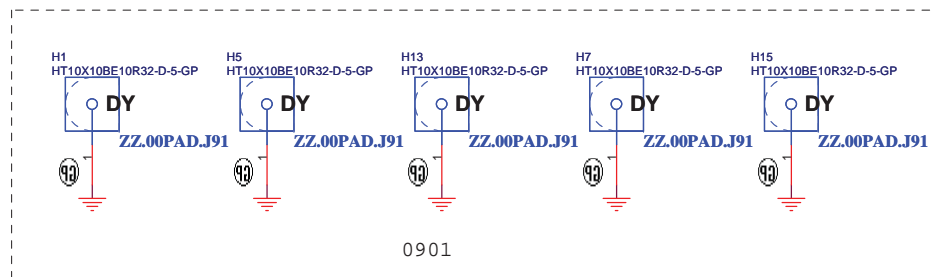


CPU Thermal module hole



stand off

0721 Modify:  
Removed SPR1

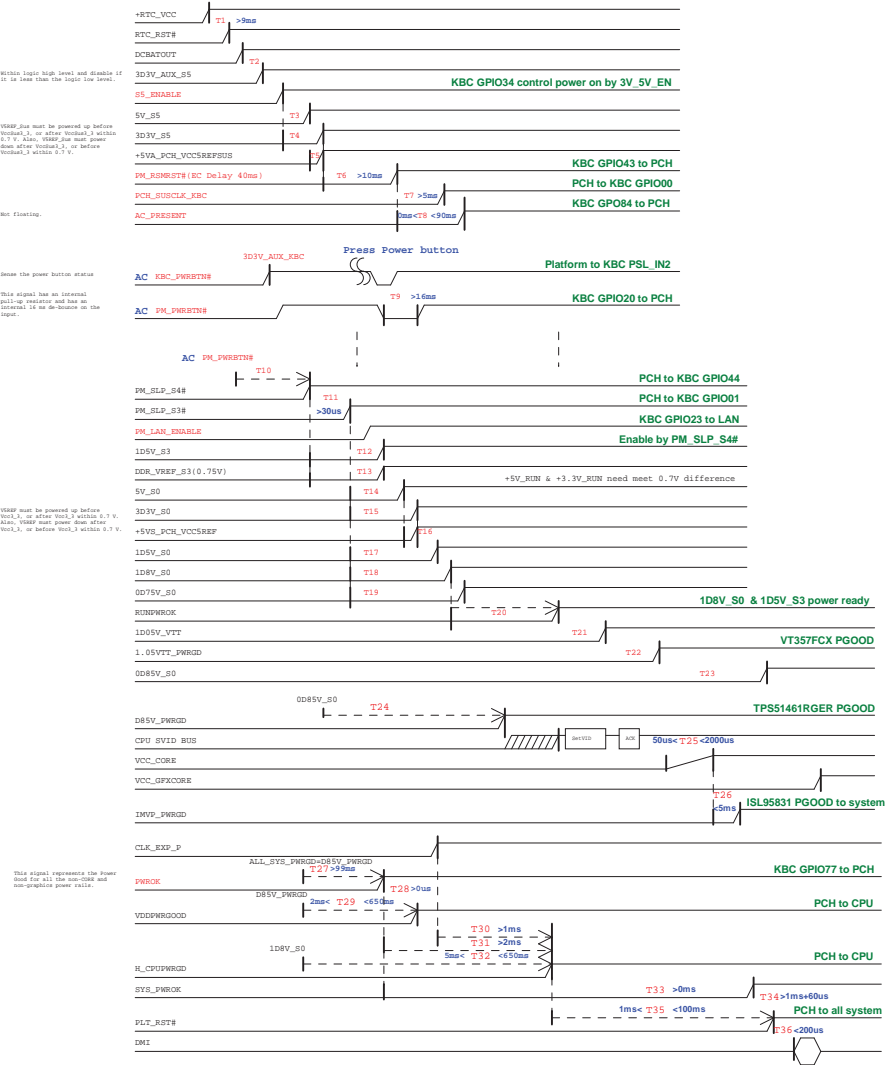


<Variant Name>

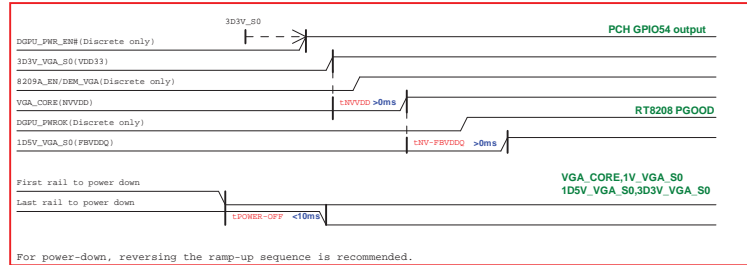
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>UNUSED PARTS/EMI Capacitors</b>		Rev <b>A00</b>
Size A3	Document Number <b>QUEEN 15</b>	
Date Tuesday, January 04, 2011	Sheet 97	of 108

red word: KBC GPIO

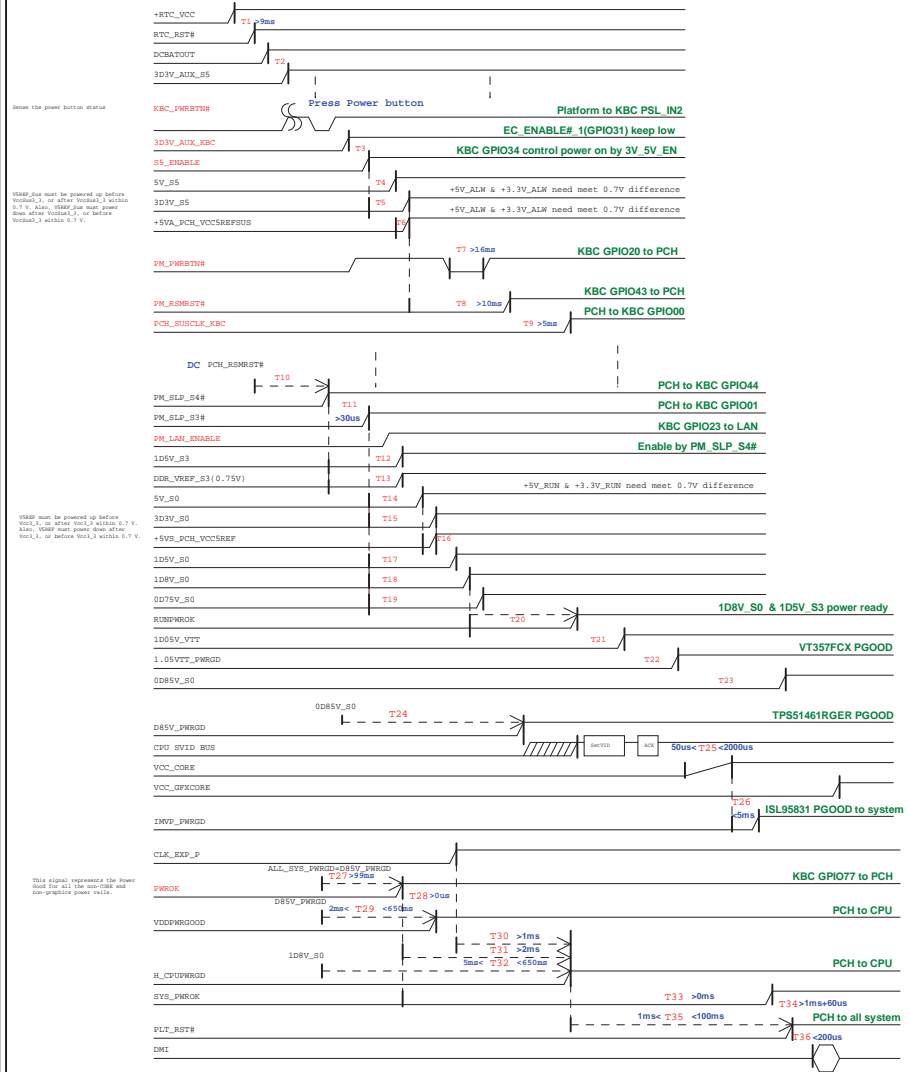


#### N12P-GE Power-Up/Down Sequence

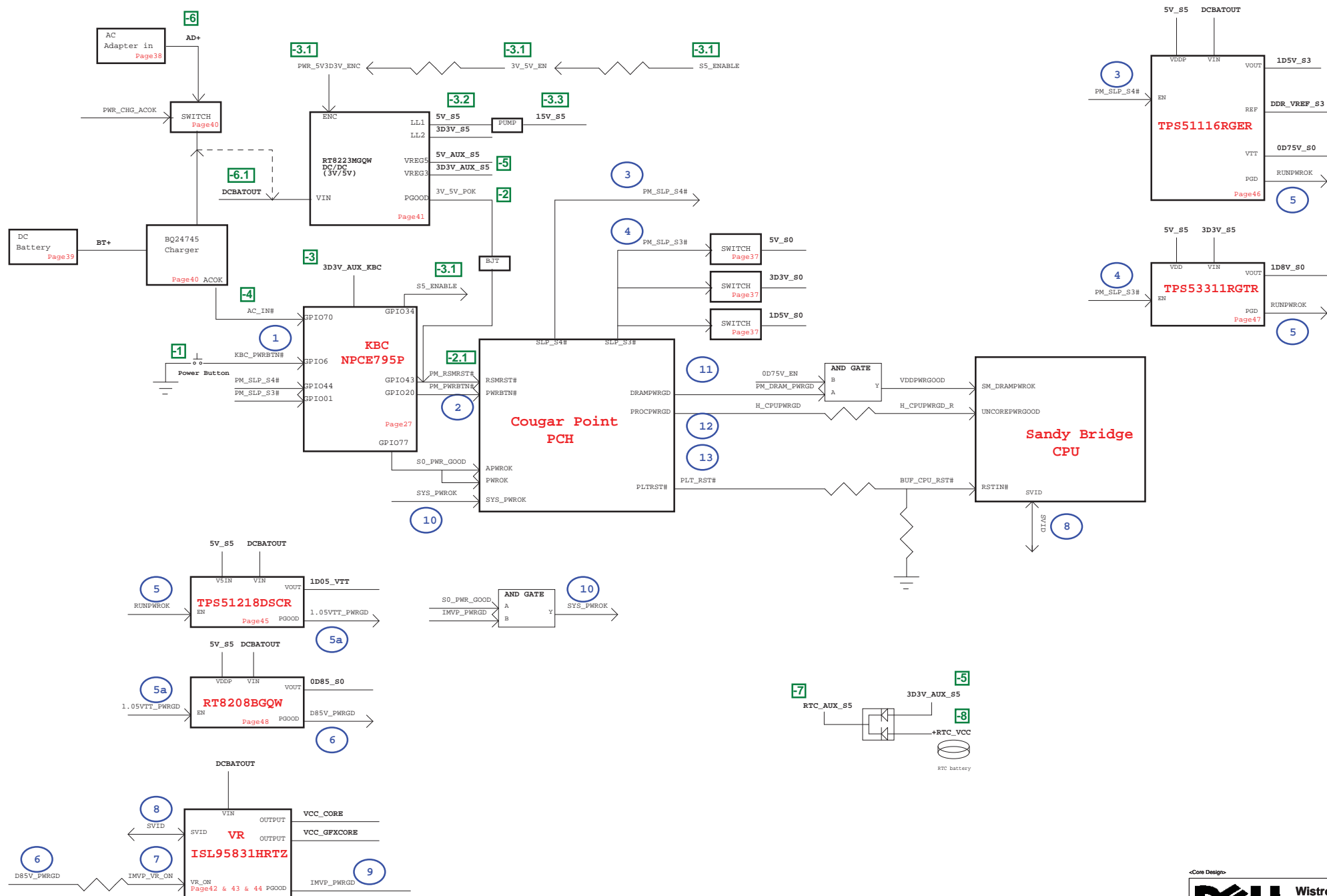


#### (DC mode)

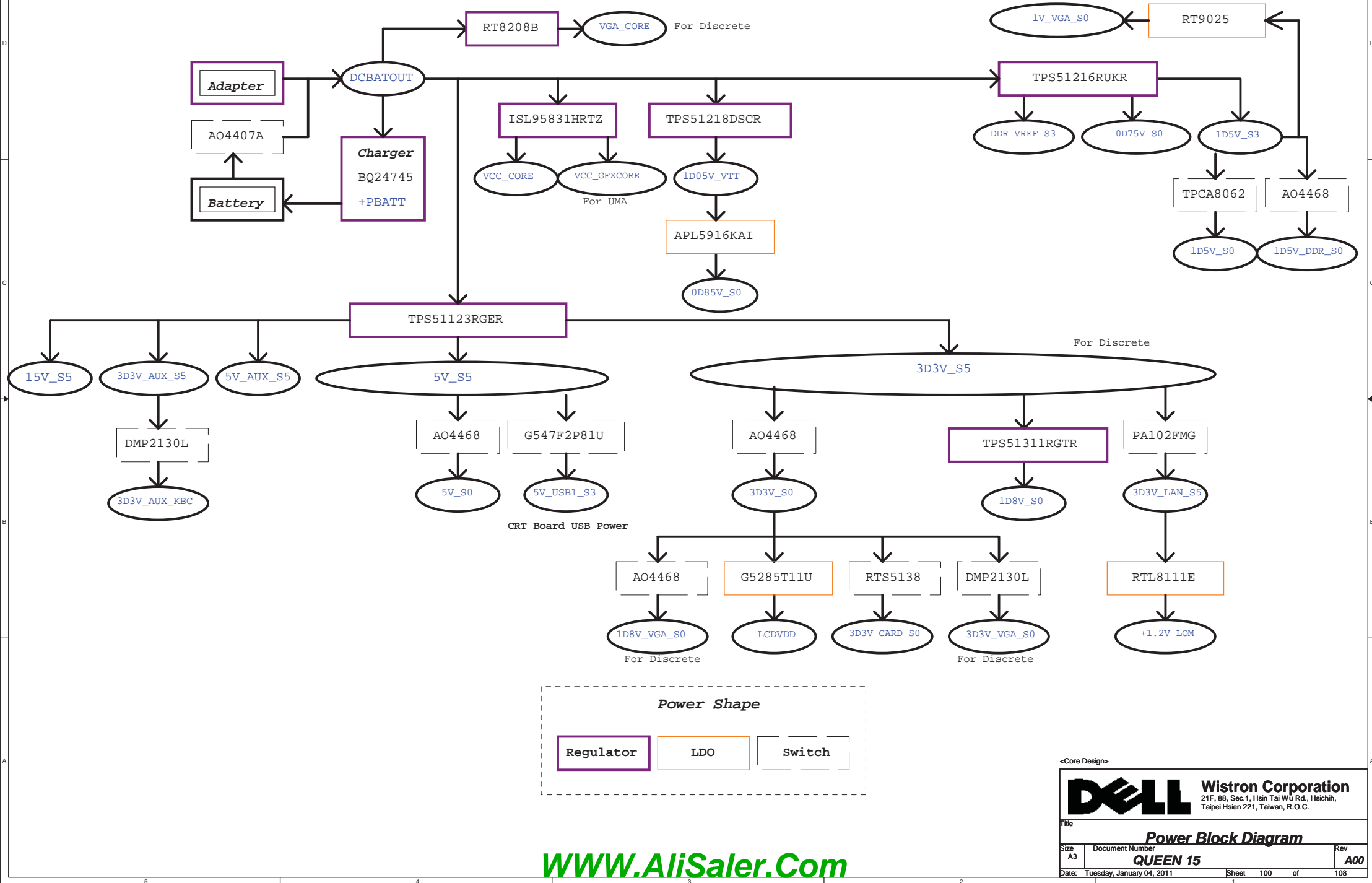
red word: KBC GPIO



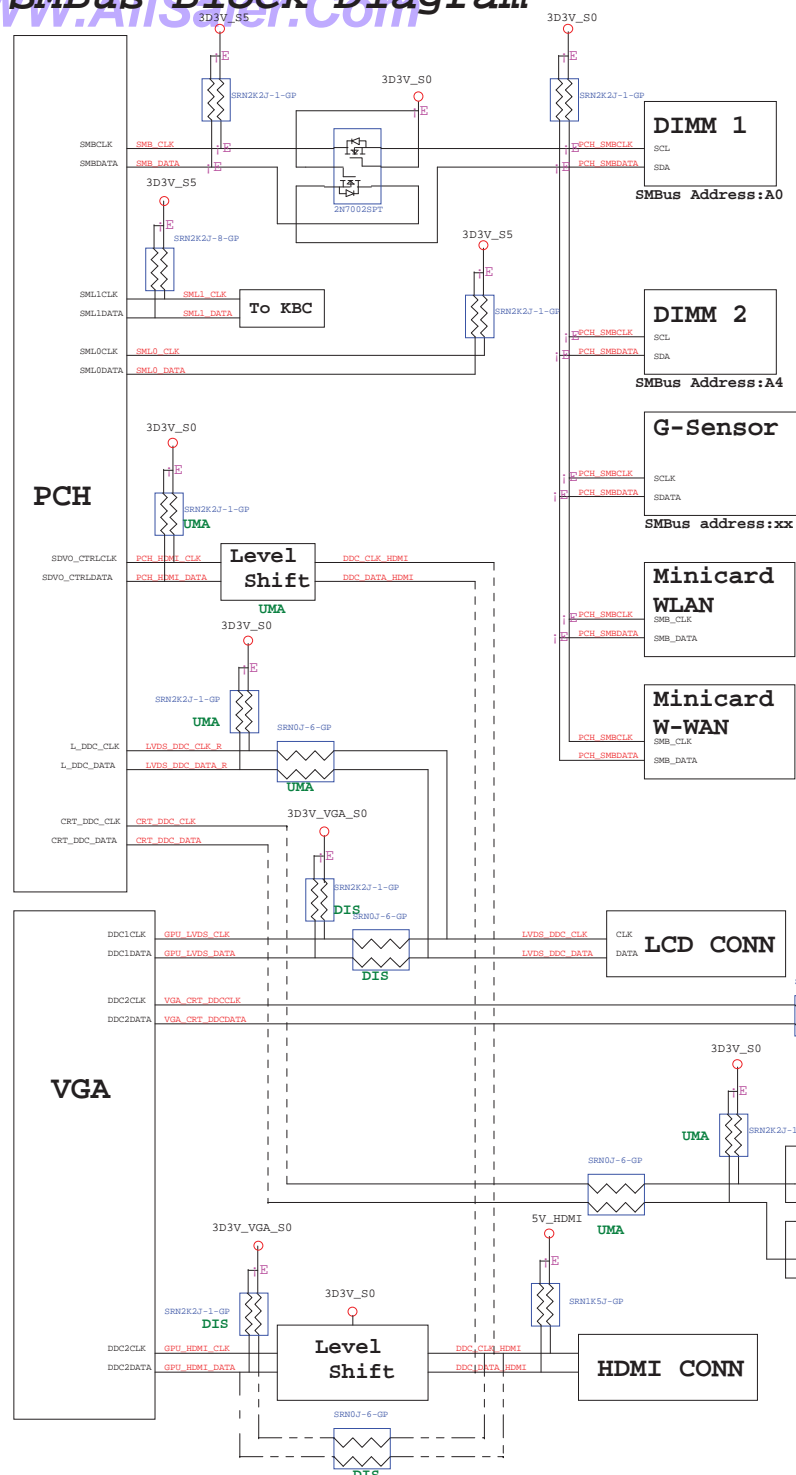
# Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



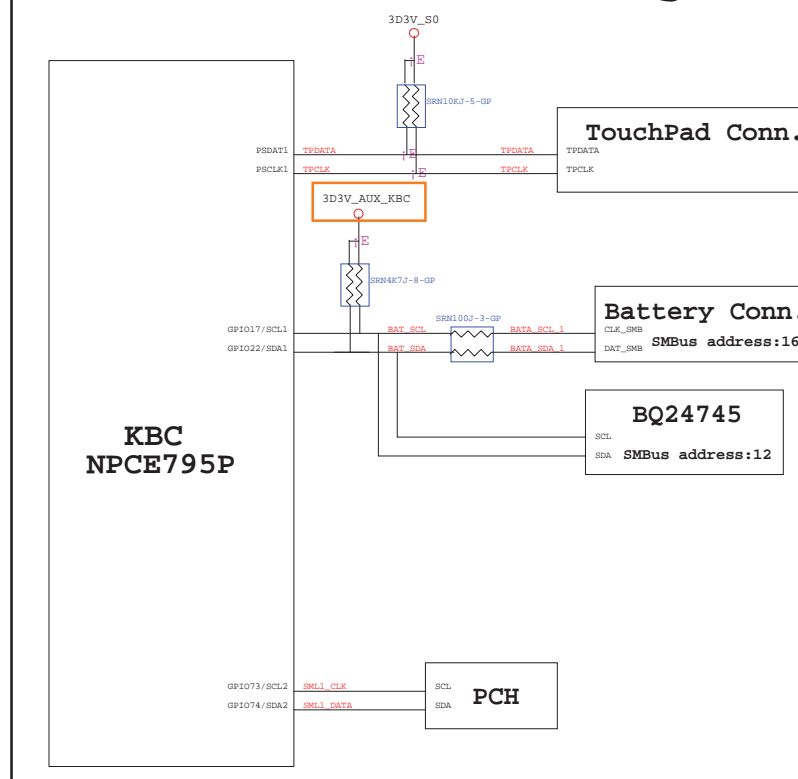
Power Up Sequence: -8 ~ 13



## PCH SMBus Block Diagram

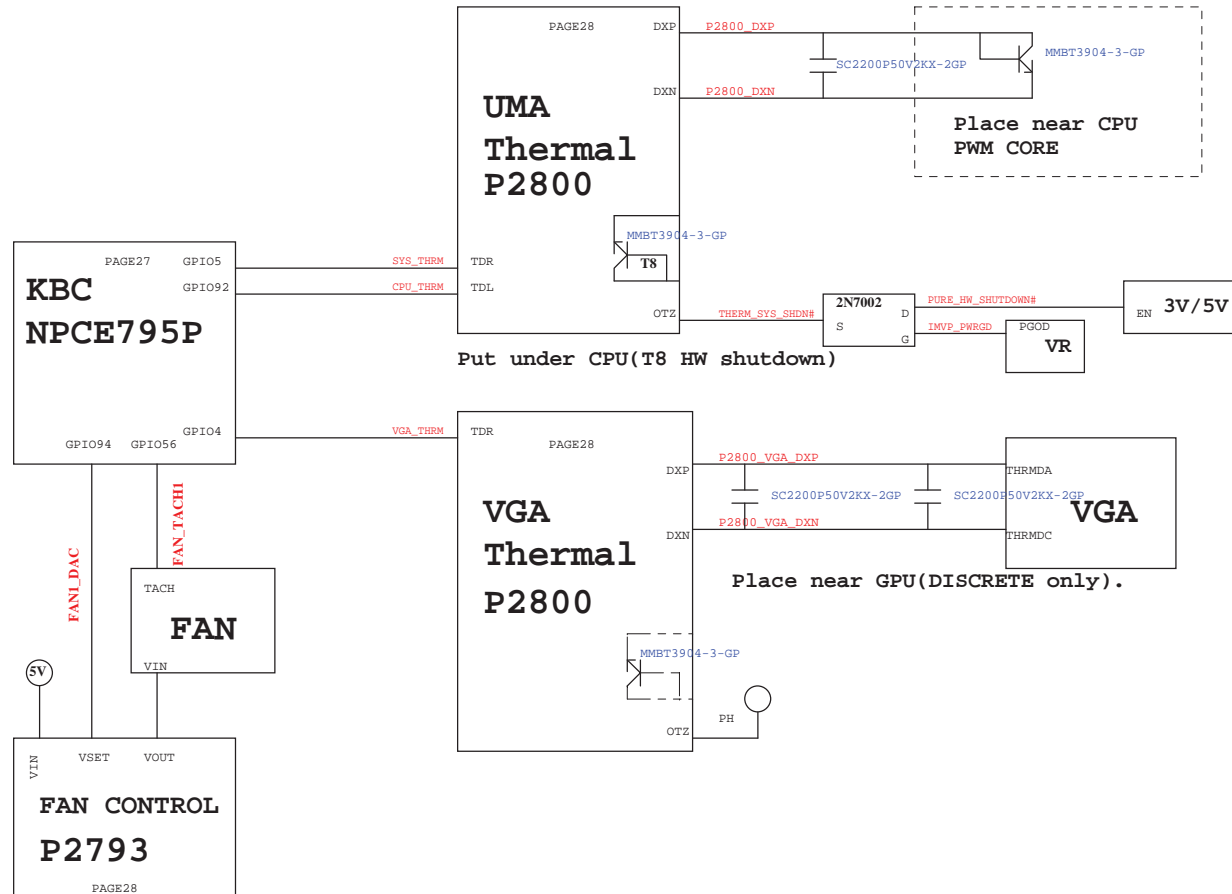


### KBC SMBus Block Diagram

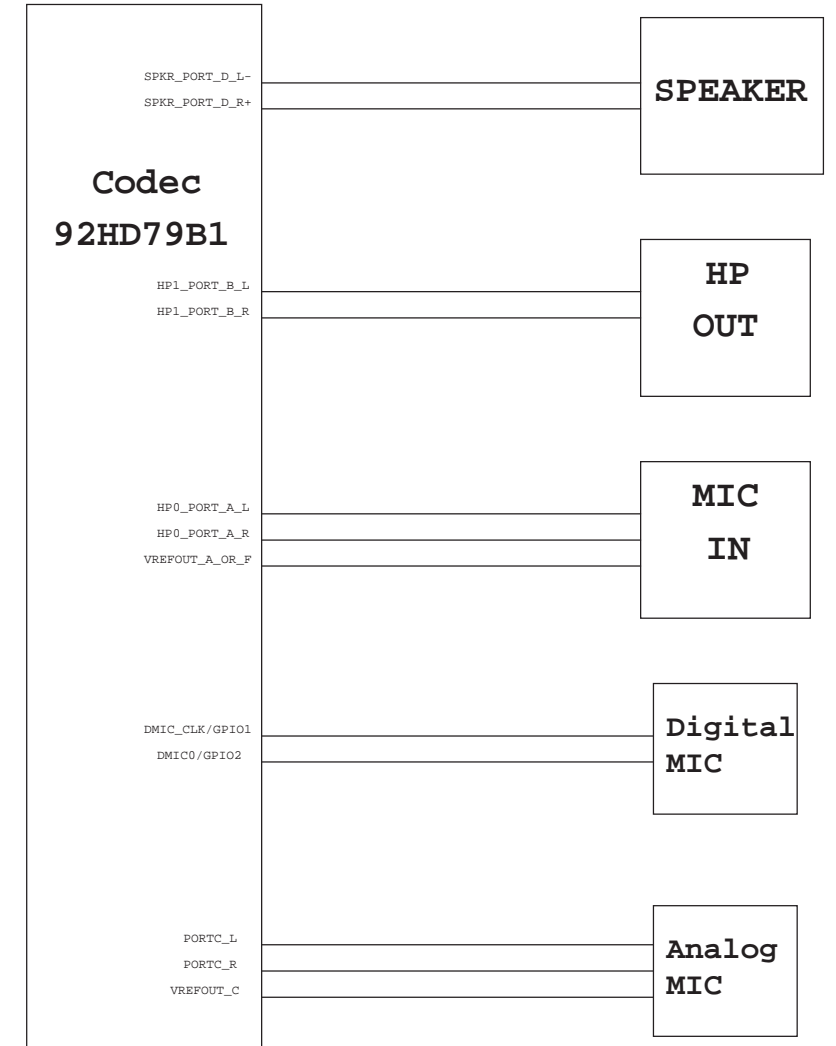




# Thermal Block Diagram



# Audio Block Diagram



<Core Design>

VERSION DATA PAGE Change Item			
X01	08/25	14	SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue.
	08/29	28	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071
	08/29	61	Add 2nd 77.C1071.20L on TC6101.
	08/29	64	Re-assign FP1 pin define.
	08/29	71	Un-stuff Debug port connector(DB1) on X01.
	08/29	37	Change U3701 pin2 to RUNPWROK from 0D75V_EN. Reserved R3717 0ohm between PM_DRAM_PWRGD and VDDPWGOOD_R.
	08/29	37	Change R2724 to 20K 0402 from 10K for X01 stage.
	08/29	40	Change 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid leakage Voltage to 3D3V_AUX_KBC under DC mode.
	08/31	51	HDMI1 change to 22.10296.311 from 22.10296.271
	08/31	28	FAN1 change to 20.F0772.003 from 20.F1639.004
	08/31	57	E-SATA1 change to 22.10321.W11 from 22.10290.141
	09/01	41	PU4104 and PU 4105 horizontally mirror.
	09/01	83	R8305 Change to 30K ohm.
	09/01	97	H1, H5, H13, H7 and H15 change to ZZ.00PAD.J91 from ZZ.00PAD.D01.
	09/01	56	HDD1 add 2nd=62.10065.121.
	09/01	79	U7901 change main source to 74.00351.0B3.
	09/01	42	PR4226 change to 5.62K ohm.
	09/01	45	PTC4502 change to 79.3971V.30L.
	09/03	61	U6101 add 2nd=74.00547.079.
	09/03	49	U4901 add 2nd=74.09724.09F.
	09/03	40	PU4002 and PU4003 add 2nd=84.P1403.B37.
	09/03	24	L2401,L2402,L2403 add 2nd=68.10090.10B.
	09/03	27	DY C2713. Add C2722.
	09/03	47	Add PR4702
	09/03	22	Change FFS_INT2_R from PCH GPIO48 to GPIO15 Removed R2220 and change R2201 default pull up to pull down.
	09/06	20	X2001 add 3rd=82.30020.A31.
	09/06	56	U5601 add 2nd=74.02191.079.
	09/06	93	PU9303 add 2nd=74.05930.03D.
	09/06	37	U3701 add 2nd=73.7SZ08.DAH.
	09/06	23	Add 2nd and 3rd for L2301.
	09/06	23	R434 change name to PR9321. Add PC9324 and PR9319 for soft start.
	09/06	61	TC6101=80.10715.B1L, 2nd=77.C1071.21L., 3rd=77.C1071.20L.
	09/06	56	ODD1 add 2nd and 3rd source. HDD1 add 3rd source.
	09/06	49	LCD1 add 2nd source.
	09/06	69	TPAD1 add 2nd.

VERSION DATA PAGE Change Item			
X01	09/06	15	DM1 2nd=62.10017.Q31, 3rd=62.10017.K01.
	09/06	14	DM2 2nd=62.10017.P31, 3rd=62.10017.K11.
	09/07	68	Add 2nd source 20.K0343.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/07	69	Add 2nd source 20.K0343.004 on KBLIT1 base on updated connector list.
	09/07	82	Add 2nd source 20.F0085.040 on CRTBD1 base on updated connector list.
	09/07	64	Add 2nd source 20.K0382.006 on FP1 base on updated connector list.
	09/07	75	Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.
	09/07	4~10	Updated CPU1 footprint to SKT-BGA989C470395-1H180 from SKT-BGA989C470395-1H186 base on data base updated. Add 2nd source 62.10040.771 on CPU1 base on updated connector list.
	09/07	75	Change CARD1 to 20.10129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.
	09/07	93	PQ9308 change name to PQ9311.
	09/07	ALL	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
	09/07	28	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K,R2804&R2818 to 226K from 102K base on updated ADJ Table.
	09/08	18, 22	Change FFS_INT2_R from PCH GPIO48 to GPIO14 Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220. Add R1818.
	09/08	82	1.Rename IOBD1 pin20,22,26,28 to IOBD1_20,22,26,28 from PCIE_TXN5,PCIE_TXP5,PCIE_RXP5,PCIE_RXN5. 2.Add RN8207,RN8208 for optional USB3.0 PCIE or USB2.0 signal.
	09/08	18	Reserved USBP9~USBP10 to IOBD1 pin20,22,26,28.
	09/08	37	Stuff Q3704,R3710; un-stuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
	09/08	20	DY R2002.
	09/08	47	Mount PC4710.
	09/08	98	Update N12P power sequence.
	09/09	82	R8201, R8202 and R8203 change to 62 ohm.
	09/10	45	Change PL4501 to 68.2R210.20C' from IND-D56UH-27-GP base on Brian updated.
	09/10	41	Change PL4101,PL4102 to 68.2R210.20B from 68.2R210.20Q base on Brian updated.
	09/10	82	Rename IOBD1 pin14 to IOBD1_14 from USB30_SMI#. Add R8207 for USB20 USB_OC#10_11 Add R8206 for USB30 USB30_SMI# Add R8208 for USB20 USB signal. Add R8207 for USB30 PCIE signal.
	09/10	49	Add TPNL1 for touch panel solution 4pin connector. Change LCD1 to 20.F1816.030 for 30pin Re-assign LCD1 pin define base on Roy updated cable pin define list.
	09/10	51	Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.

DELL

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size A3

Document Number QUEEN 15

Rev A00


Date: Tuesday, January 04, 2011

Sheet 103 of 108

VERSION	DATA	PAGE	Change Item
X01	09/13	83	Change X8501 to 82.30034.641;2nd 82.30034.651;3rd 82.30034.681 from sourcer suggestion.
	09/13		Change KBLIT1, PWRBTN2 and TPAD1 2nd source from 20.K0343.004 to 20.K0382.004.
	09/13	47	Change 1.8V power solution.
	09/14	82	Change R8201~R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.
	09/14	40	Add 2nd source 84.04835.H37 on PU4002,PU4003 base on Brian updated 2nd source excel file.
	09/14	58	Change SPK1 to 20.F0772.004 from 20.F1647.004 from Double updated.
	09/14	51	Add R5101~R5108and reserved TR5101~TR5104 on all of HDMI differential pair for EMC suggestion. Rename HDMI1 CONN NET name.
	09/14	29	Add R2920,R2921 and reserved EC2901,EC2902 on AUD_DMIC_CLK &AUD_DMIC_IN0 for EMC suggestion.
	09/14	75	Add R7503,R7504 and reserved EC7501,EC7502 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion. Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R. Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C
	09/14	20	Reserved EC2004,EC2005 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
	09/14	49	Reserved EC4910~EC4915 on LVDS signal for EMC suggestion.
	09/15	58	Re-assign SPK1 pin define base on Roy updated excel file for 20.F0772.004
	09/15	51	Add 2nd source 22.10296.311 on HDMI1 from updated connector list.
	09/15	68	Add 2nd source 20.K0382.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	49	Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.
	09/15	28, 51,82	Add test point for WKS AFTE request.
	09/15	All	ADD 2nd source follow Power team suggestion.
	09/15	92, 93	Modify PR9318 and PR9228 power source from 3D3V_AUX_S5 to 3D3V_S5.
	09/15	86	Reserve Q8602, C8603 and R8606 for VGA over temp.
	09/15	20	RN2005 swap net.
	09/15	19	RN2005 swap net.
	09/15	48	Change PR4809 to 10K from 100K PH power source change to 3D3V_S0 from S5.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	97	Reserved EC9701~EC9723 0.1uF for RF suggestion.
	09/15	41	Un-stuff PU4101,PD4105,PR4124, PR4125,PR4101 at X01 stage for 5mW issue.
	09/15	69	un-stuff R6907 and stuff R6905,Q6902,R6906 for 5V drive CAP LED.
	09/17	82	Change IOBD1 part number to 20.F1849.080 base on Double updated latest DXF&EMN.
	09/17	49,57 32,64	stuff TR4901 and un-stuff R4911,R4912 at X01 stage from EMC Neo suggestion. stuff TR4902 and un-stuff R4908,R4909 at X01 stage from EMC Neo suggestion. stuff TR5701 and un-stuff R5718,R5719 at X01 stage from EMC Neo suggestion. stuff TR3201 and un-stuff R3211,R3210 at X01 stage from EMC Neo suggestion. stuff TR6401 and un-stuff R6403,R6404 at X01 stage from EMC Neo suggestion.
	09/17	20	Change RN2010~RN2016 to 33ohm from 0ohm from EMC Neo suggestion.
	09/17	37	Change R3710 to 100K from 0ohm to avoid impact I.05VTT_PWRGD turn off sequence directly.
	09/17	17	Add R1703~R1705 on RGB signal and reserved EC1701~EC1703 0.1u from EMC Neo suggestion.

VERSION	DATA	PAGE	Change Item
X01	09/17	40,41	Stuff EC4002 0.1uF from EMC Neo suggestion. Stuff EC4008 0.1uF from EMC Neo suggestion. Stuff EC4102,EC4103 0.1uF from EMC Neo suggestion. Stuff EC4107 0.1uF from EMC Neo suggestion. Stuff PC4119,PC4120 0.1uF from EMC Neo suggestion. Stuff EC4006,EC4007 0.1uF from EMC Neo suggestion.
	09/17	60,18	EC6001 change to 10p from 4.7p and default stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default stuff from Neo suggestion.
	09/17	44	default stuff EC4407,EC4405,EC4403,EC4410 base on EMC Neo suggestion.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	82	Change R8201~R8203 to 430ohm.
	09/17	48	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
	09/17	40,27,83	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037 for AD_IA_HW2 function.
	09/17	68	Rename CHARGER_LED1 to CHARGERLED1. Rename FPOWER_LED1 to FPOWERLED1. Rename HDD_LED1 to HDDLED1. Rename TP_LOCK_LED1 to TPLOCKLED1. Rename TP_LOCK_LED2 to TPLOCKLED2. Rename WLAN_LED1 to WLANLED1
	09/17	21,22	Base on layout routing,Add RN2104 10K instead of R2111 10K. Move EC_SCI#,DBC_EN to RN2201. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
	09/17	56	Change R5605 to 100K from 10K and PH to 5V_S0 from 3D3V_S0 to meet Vgs>2V turn on.
	09/17	56	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
	09/17	ALL	Change all of 0402 0ohm to 0R0402 short pad. PR4008,PR4010,PR4012,PR4020,PR4023,PR4024,PR4027,PR4028,PR4029,PR4225PR4102,PR4113,PR4118, PR4121,PR4203,PR4204,PR4215,PR4222,PR4231,PR4243,PR4301,PR4509,PR4510,PR4801,PR4804,PR4805, PR4808,PR4810,PR9211  F4902,PR4017,PR4018,PR4106,PR4611,PR4710,PR4807,R2304,R2403,R2406,R2409,R2702,R2902,R2903,R2904 R2305
	09/20	9	Add 2nd for TC901.
	09/20	83	Add 2nd for L8303.
	09/20	82	Add 2nd for LD8201.
	09/20	86	Add 2nd for Q8601.
	09/20	83	Add R8321. C8353 and C8354 change to 12pF.
	09/20	82	Redefine IOBD1.
	09/20	75	AFTP111 and AFTP110 connect to USB_PP13_R and USB_PN13_R.
	09/20	51	Change P/N of Q5102.
	09/21	42	Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.
	09/21	47	stuff PC4714 22uF from Brian updated.

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


**Change History**

Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 104 of 108	

VERSION	DATA	PAGE	Change Item
X01	09/21	45	Change PR4507 to 20K from 20.5K from Brian updated.
	09/21	46	Change PR4602 to 110K from 68K from Brian updated.
	09/21	42	Change PR4217 to 1.27K from 1K from Brian updated. Change PR4213 to 3.6K from 3.16K from Brian updated. Change PR4236 to 3.01K from 3.32K from Brian updated.
	09/21	44	Change PC4410 to 0.01u from 0.022uF from Brian updated.
	09/21	39	Add 2nd 83.00099.K11;3rd 83.00099.T11 on D3901,D3902,D3903 from Sourcer Eden suggestion.
	09/21	39	Add 2nd 84.02143.011;3rd 84.00143.N11 on 6801,Q6804,Q6805,Q6806,Q6807,Q6808 from Sourcer Eden suggestion.
	09/21	43	Change PU4303,PU4306,PU4309 dummy field only for QC CPU stuff. Change PC4307,PC4316 dummy field only for QC CPU stuff. Add 2nd for PTC4306.
	09/21	41	PD4101, PD4103, PD4104 and PD4105 add 2nd source.
	09/21	69	Q6902 add 2nd source.
	09/21	40	PD4001 add 2nd source.
	09/21	19	move PCH_WAKE# to RN1901 pin4;Add R1909 PH 100K on AC_PRESENT.
	09/21	37	R3710 change to 0ohm. Remove R3701 and C3701.
	09/21	42	Add PR4214, PC4230, PR4216 and PC4231 from Brian updated.
	09/23	20	RN2016, RN2010, RN2011, RN2012, RN2014 and RN 2013 keep 0ohm.
	09/23	ALL	PR9216, R504, R1812,R1813,R1815,R1817, R1903, R1906,R1910,R1912,R1913,R1924,R1925, R2213,R2219, R2711,R2720,R2733,R2761, R2807,R2814, R3708, R5125, R5127, R5721, R5722.
	09/23	75	Add R7505~R7508 0ohm and reserved EC7503~EC7506 on PCIE_TX8&RX8 signal base on EMC Lance suggestion. Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base on EMC Lance suggestion.
	09/23	ALL	RN5101, RN2201, RN1702, RN1901, RN1705 swap pin.
	09/23	79	DUMMY G-SENSOR.
	09/23	92	Update value of PR9210, PR9209 and PR9213 for N12P.
	09/23	43	PR4320 change to 4 m ohm.
	09/23	68	Add 2nd source 83.00110.J70 on FPOWERLED1,HDDLED1,WLANLED1 from Sourcer Anya suggestion. Add 2nd source 83.00326.G70 on CHARGERLED1from Sourcer Anya suggestion. Add 2nd source 83.00190.Z70 on TPLOCKLED1,TPLOCKLED2 from Sourcer Anya suggestion.
	09/23	69	Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.
	09/23	42, 44	Add 2nd source 69.60011.201 on PR4405,PR4245 from Sourcer Kitty suggestion.
	09/23	42	Add 2nd source 69.60037.021 on PR4246,PR4247 from Sourcer Kitty suggestion.
	09/24	23	Add 2nd source 68.00214.211 on L2301 updated from DN13ATI.
	09/24	68, 69	Change R6806,R6808,R6811~R6813,R6801,R6803,R6815,R6906 to 390ohm from 1K to fine tune all of MB LED for 5mA spec.
	09/27	51	Reserve R5114 and R5115.
	09/27	85	Reserve R8510 and R8513.
	09/27	83	DY U8301, mount R8323.
	09/27	92	R9206 change to 10K, PC9211 mount 0.1u.
	09/27	93	R9312 change to 1K.

VERSION	DATA	PAGE	Change Item
X01	09/27	49, 57 32, 64	TR4901, TR4902, TR5701, TR3201 and TR6401 DY. Stuff 0 ohm.
	09/27	69	AFTP73 connect to TP_VDD.
	09/27	85	U8501 power change to 3D3V_S0.
	09/27	92	PL9201 change like CPU core power choke.
	09/28	83, 84	L8303, L8401, L8402, L8502 and L8503 follow NV DG spec.
	09/28	46	Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.
	09/28	92	PTC9202, PTC9203 and PTC9204 2nd=79.47719.9BL
	09/28	22	Change R2220 to 10K from 100K.
	09/28	60	EC6001 change to 10p from 4.7p and default un-stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default un-stuff from Neo suggestion
	09/28	27	Change R2710, R2739, R2724 and R2726 change to 1%.
	09/29	27	Default mount R2756, Dummy R2734.
	10/04	24	Add 2nd source 68.1001E.10N on L2401,L2402,L2403 from sourcer Renee Lee updated.
	10/07	43	PTC4306 cahnge second source to 79.47612.60L.
	10/09	85	Change L8503 to 68.00375.091,and add second source 68.00206.171
	10/09	85	Change L8502 to 68.00115.191,and add second source 68.00206.131
	10/09	84	Change L8401 and L8402 to 68.00115.181,and add second source 68.00206.341
	10/09	83	Change L8303 to 68.00375.101,and add second source 68.00119.101
	10/09	83	Change L8301 to 68.00115.161,and add second source 68.00206.111
	10/09	42	Change PR4217 to 64.84505.6DL for Dual-core OCP
	10/09	42	Change PR4213 to 64.23715.6DL for Dual-core loadline
	10/09	42	Change PR4207 to 64.22025.6DL for CPU(35W) Turbo setting
	10/09	42	Change PR4202 to 64.22025.6DL for GFX Turbo setting
	10/09	20,83	Dummy R2004 R2003 and PQ8309, stuff R2005
	10/19	28	Change R2817 from 107K to 124K (64.12435.6DL) for VGA temperature setting change
	10/25	84	Change R8402 from 40D2R to 60D4R (64.60R45.6DL) for meeting the spec
	10/25	14 15	Add DM1 and DM2 second source:62.10017.Q41 and 62.10017.P61
X02	10/25	85	Ventura SMBC_INA219_C and SMBD_INA219_C add 3.3V pull high schematic
	11/01	51 85	Change HDMI HPD schematic for cost down
	11/10	27	Change R2724 to 64.33025.6DL for PCB version change
	11/10	83	Change L8301 to 68.00115.181,and add second source 68.00206.341

<Core Design>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size A3

Document Number  
QUEEN 15

Rev  
A00


Date: Tuesday, January 04, 2011

Sheet 105 of 108

VERSION	DATA	PAGE	Change Item
X02	11/11	14	DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.
	11/11	15	DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.
	11/11	60	U6001 1st change to 72.25Q32.A01; 2nd change to 72.25320.C01; 3rd change to 72.25P32.C01 on ST stage
	11/11	68	Change CHARGERLED1 2nd to 83.00327.D70 from Sourcer updated.
	11/11	37	Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.
	11/11	69	Add 2nd 20.K0592.030 on KB1 from ME updated connector list.
	11/11	82	Add 2nd 20.K0465.008 on MEDIA1 from ME updated connector list.
	11/11	58	Add 2nd 20.F1804.004 on SPK1 from ME updated connector list.
	11/11	28	Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
	11/11	70	Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.
	11/11	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0.
	11/11	60	Add Q6002,R6007 fo FACTORY RTC detect function
	11/11	28	ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
	11/11	28	Reserved G709T1UF for T8 solution sync with DN13.
	11/12	82	Change R8201, R8202, R8203 from 430 ohm to 1K ohm (63.10234.1DL) for soluting media board LED brightness is too light issue
	11/15	49	Add 2nd 20.F1860.030 on LCD1 from ME updated connector list.
	11/15	8	Reserved C802~C804,C806,C807 10uF 0603 for power team fine tune Vcore quality
	11/15	88 89 90 91	All of VRAM(VRAM1~VRAM8) PCB footprint change to CO-LAY type (DUMMY-BGA96D075133H48) from BGA96D0913H48 same as DW30.
	11/15	68 69	Change R6813, R6906 from 390 ohm to 1K ohm (63.10234.1DL) for soluting LED brightness is too light issue
	11/15	20	Dell required us to disable PCIE port of WWAN slot ,If PCIE port 1 is disabled, it will cause all PCIE port disabled,so change WWAN to PCIE port 3 from port1 at ST stage.
	11/16	97	Change HHD1 HDD4 HGPU1 HGPU2 2nd from 34.4CK01.201 to 34.4CK01.401 from ME update connector list
	11/16	68	Change R6808, R6811 from 390 ohm to 1K ohm (64.10234.1DL) for soluting LED brightness is too light issue
	11/16	28	stuff both G709T1UF and P2800 related circuit, add R2805 0ohm default un-stuff at ST stage.
	11/17	48	CO-LAY APL5916 related circuit for VCCSA LDO solution.
	11/18	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2301 and un-stuff L2301.
	11/18	28	Add R2805 0hm between THERM_SYS_SHDN#_ OTZ and THERM_SYS_SHDN#. Add R2812 0ohm between THERM_SYS_SHDN# and U2805 pin3.

VERSION	DATA	PAGE	Change Item
X02	11/18	28	Rename U2801&U2804 pin 8 to THERM_SYS_SHDN#_ OTZ from HERM_SYS_SHDN#.
	11/18	20	Change X2001 to 82.30020.D41 from 82.30020.851 from Sourcer Dick updated.
	11/18	23	Reserved R2308,R2309 on VCCVRM power rail.Reserved U2302 LDO circuit on VCCVRM power rail
	11/18	22 82	Rename USB3_PWR_ON to PCH_GPIO57. Add R8209,R8210 for PM_SLP_S4# and VGA_THRM to control USB3_PWR_ON
	11/18	48	Change PTC4801 to 100u(77.21071.07L) from 150u from power team Brian updated
	11/19	74	Add 2nd 20.I0135.001 on CARD1 from ME updated connector list.
	11/19	82	Add 2nd 20.F1908.080 on IOBD1 from ME updated connector list.
	11/20	3	Updated PCIE ROUTING
	11/20	28	Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2812, un-stuff R2805
	11/20	23	Reserved R2308 on VCCVRM power rail. Reserved U2302 LDO circuit on VCCVRM power rail.
	11/20	48	Set TPS51461 PWM solution dummy field for VCCSA_PWM and APL5916 LDO solution dummy field for VCCSA_LDO. default stuff VCCSA_LDO at ST stage
	11/20	22	Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.
	11/20	60	Un-stuff R6007 10M.
	11/20	82	Reserved EC8201,EC8202 0.1u(closed H3) between AGND and GND from EMC Neo suggestion.
	11/20	82	Reserved EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/20	82	Add RN8205 base on HSYNC&VSYNC report
	11/20	61	Removed R6101 and connect USB_PWR_EN# to U6101 pin4 directly.
	11/20	22	Rename PCH_GPIO12 to RTC_DET# on GPIO12.
	11/20	61 22 18	Reserved U6102 USB POWER related circuit to separate EATA and CRT USB power in ST build. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/20	82	Reserved R8211,R8212 0ohm 0805 on CRTBD1 pin37,39 to separate EATA and CRT USB power in ST build.
	11/22	82	Swap RN8205 pin4,3 and pin2,1 each other base on Connie swap report.
	11/22	82	stuff EC8201,EC8202 0.1u(closed H3) between GND and GND from EMC Neo suggestion. stuff EC8206 between 3D3V_S5 and GND from EMC Neo suggestion.
	11/22	23	base on layout condition change 3D3V_DAC_S0 circuit. Stuff R2301 and un-stuff L2301.
	11/22	82	stuff EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/22	23	Removed U2302 LDO for VCCVRM.


<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Change History</b>					
Size A3	Document Number <b>QUEEN 15</b>				Rev <b>A00</b>
Date: Tuesday, January 04, 2011		Sheet 106		of 108	

VERSION	DATA	PAGE	Change Item
X02	11/22	29	change R2920,R2921 to 22ohm from 0ohm and stuff EC2901,EC2902 22p from EMC Neo updated.
	11/22	61	Change U6101 to dual USB power switch from single for Layout limitation and placement. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/22	49	stuff C4908 0.1uF from EMC Neo suggestion.
	11/22	57	Change TR5701 to 69.10103.041 and un-stuff R5718,R5719 from EMC Neo Suggestion.
	11/22	49	Change TR4902 CM choke to 69.10103.041 and un-stuff R4908,R4909 from EMC Neo Suggestion.
	11/22	49	Swap TR4901 pin4,3 and pin2,1 each other base on Connie swap report. Change TR4901 CM choke to 69.10103.041 and un-stuff R4911,R4912 from EMC Neo Suggestion.
	11/22	75	Change TR7501 CM choke to 69.10103.041 and un-stuff R7501,R7502 from EMC Neo Suggestion.
	11/22	58	stuff EC5801~EC5804 470pF from EMC Neo suggestion.
	11/22	9 39 45 49	stuff EC901, EC3903, EC4501, EC4909, EC4907 0.1uF from EMC Neo suggestion.
	11/22	49	Change RN4901 to 100ohm 4p from 8p for improve layout place.
	11/22	48	Updated VCCSA_LDO circuit from Power team Brian updated.
	11/22	83 84 85	Change L8301 L8401 L8402 to 0 ohm resistor (63.00000.00L)
	11/22	60	stuff R6007 10M.
	11/23	49 57 75	SWAPTR4901 TR4902 TR5701 TR7501 pin1&4 and pin2&3 each other base on Connie swap report.
	11/23	60	Change U6101 1st(74.02182.071);2nd(74.00546.A7D);3rd(74.02062.079) from Sourcer Harrison suggestion.
	11/23	64	Add C6402 0.1uF,C6403 180pF and stuff C6401 47pF from RF fine tune result.
	11/23	57 49 75	Change R5718,R5719,R4908,R4909,4911,R4912,R7501,R7502 to 0ohm 0603 from 0402.
	11/23	56 97	stuff EC9739,EC9737,EC9735 47pF from RF fine tune result. stuff EC5601 180pF from RF fine tune result. Stuff EC9738 0.22uF closed EC9739 from RF fine tune result.
	11/23	97	stuff ECEC9729,EC9730 470pF from EMC Neo suggestion.
	11/23	45	Change PR4501 to 75K from 45.3K for 1.05V OCP set to 20A from Brian.
	11/23	82	Removed R8211,R8212 and connect 5V_USB2_S3 to CRTBD1 pin 37 directly.
	11/23	61	Removed C6105,C6103.
	11/23	69 70	Change AFTP 80 81 to AFTP 83 84; change AFTP 83 to AFTP82; change AFTP 82 to AFTP85.
	11/24	20	Add 2nd(82.30020.G71);3rd(82.30020.G61) on X2001 from Sourcer Dick updated.
	11/24	69	Add 2nd(20.K0613.004)on KBLIT1 from Karl updated.

VERSION	DATA	PAGE	Change Item
X02	11/24	57	Add 2nd(22.10339.261)on ESATA1 from Karl updated.
	11/24	28	un-stuff VGA P2800 related circuit from Niki confirmed.
	11/24	64	rename C6401,C6402,C6403 to EC6401,EC6402,EC6403
	11/24	22	Dummy R2206
	11/25	28	Dummy R2817 R2818 C2816
	11/25	69	Add 3rd(83.00110.R70) on FPOWERLED1,HDDLED1,WLANLED1 from Anya provide
	11/25	69	Add 3rd(83.00192.J70) on TPLOCKLED1 and TPLOCKLED2 from Anya provide.
	11/25	69	Add 3rd(83.01108.070) on CHARGERLED1 from Anya provide.
	11/26	43 92	Change PC9217 PC4319 to 0.1u 50V
	11/29	83	Change C8353 C8354 to 15PF ,R8320 stuff from vendor suggestion.
	11/29	36	Stuff D3602
	11/30	68	Change 2nd source to 83.00322.070 from 83.00110.J70
	11/30	85	Change L8502 L8503 to 0 ohm
	11/30	92	Stuff PR9237 DY PR9321
	12/01	8	Change C837,C826 to 22uF from 10uF and default stuff from Power Brian updated.
	12/01	8	Change C801~C807 and C817 10uF stuff at QC CONFIG from power Brian updated.
A00	12/21	ALL	Change 0402 pad(ZZ.00PAD.M11): R1404 R1405 R1503 R1504 R1703 R1704 R1705 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R2762 R3614 R3710 R5114 R5801 R5802 R5803 R5804 R8210 R8323 R8511 R8512
	12/21	82	Change 0603 pad(ZZ.00PAD.M21): R8206 R8207
	12/21	17 20	Change resistor pad(ZZ.0R04P.ZZZ): RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2015 RN2016
	12/21	83 84 85	Change L8301, L8401,L8402,L8502,L8503 to 0R0603 pad(ZZ.00PAD.M21)
	12/21	ALL	Change to Parallel resistor R1501 ,R1502; R2739 ,R2774;R8202 ,R8203;R8501 ,R8502;R8506 ,R8507;R2123 ,R2124
	12/21	82	RN8205 change to R8201, R8202
	12/21	93	PR9237 rename to PR9337
	12/21	56 61 68	Delete 77.C1071.21L(TC6101), delete 83.01108.070(CHARGERLED) , delete 62.10065.121(HDD1)

<Core Design>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size A3

Document Number

Rev

Date: Tuesday, January 04, 2011


Sheet 107 of 108

A00

VERSION	DATA	PAGE	Change Item
A00	12/22	27	R2724 change to 47K resistor for XBuild
	12/22	27	R2301 change to 0 resistor for CRT debug
	12/22	40	1.Change PR4032,PR4034,PR4037 to ZZ.00PAD.M11 2.Stuff PQ4003,PQ4004 3.Change PR4047 to 174K(64.17435.6DL) 4.Change PR4035 to 300K(64.30035.6DL) 5.Change PR4036 to 76.8K(64.76825.6DL) 6.Change PR4031 to 150K(64.15035.6DL)
	12/23	68	1.FPOWERLED1 rename to FPLED1 2.HDDLED1 rename to HDLED1 3.CHARGERLED1 renamtpe to CHLED1 4.WLANLED1 rename to WLED1 5.TPLOCKLED2 rename to TPLED2 6.TPLOCKLED1 rename to TPLED1 7.PWRBTN1 rename to PWRBT1 8.PWRBTN2 rename to PWRBT2
	12/23	43	Delete PR4323,PR4324,PR4325; Stuff PR4320 for all BOM ,not co-lay Ventura
	12/23	92	Delete PR9220,PR9222,PR9223; Stuff PR9217 for all BOM ,not co-lay Ventura
	12/23	51	Change 5V_HDMI to 5V_CRT_S0_R for HDMI power leakage
	12/24	All	PRN3901 rename to PN3901 PTC9202-04 rename to PT9202-04 PTC4301-04 rename to PT4301-04 PTC4306 rename to PT4306 PTC4308-09 rename to PT4308-09 PTC4401-03 rename to PT4401-03 PTC4502 rename to PT4502 PTC4602 rename to PT4602 PTC4102 rename to PT4102 PTC4104 rename to PT4104
	12/24	28	Change U2802 3rdto 74.05606.A71 at X-Build batch run
	12/24	82	Change RN8205 to 66.22036.04L from 66.22036.040at X-Build stage
	12/24	82	Reserved R8211 0603 0ohm on F8201
	12/24	36	Reserved Q3603 2N702 on IMVP_PWRGD to fine tune glitch waveform when AC lose and DC lose.
	12/24	28	Change 3D3V_S0 to 3D3V_DAC_S0
	12/24	45 46 93	Change to short pad: PR4502,PR4607,PR9311,PR9312,PR9326. DUMMY PC4501
	12/27	28	If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.
	12/27	42	PR4207,PR4213,PR4217 DUMMY field set to DC&QC option
	12/28	51	Change 5V_HDMI to 5V_CRT_S0_R on RN5101
	12/28	28	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at XBuild

VERSION	DATA	PAGE	Change Item
A00	12/28	27	Change R2756, R2763, R2766 to short pad
	12/28	36	Stuff Q3603
	12/28	28 86	Cancel VGA Thermal sensor P2800 circuit
	12/28	27 28 82	Change to VGA_THRM to USB3_PWR_ON
	12/28	23	Change R2301 to short pad
	12/29	51	Change HDMI resistor to short pad
	12/29	49,57,75	Delete USB DUMMY resistor for no-lay
	12/29	32	Change USB 0 resistor to short pad for no-lay
	12/29	5	Reserve EC502 ,EC504 for EMI suggestion,add DUMMY EC505 for EMI
	12/29	82	Delete PM_SLP_S4# line, directly link to USB3_PWR_ON
	12/29	23	Add 3rd Richtek(74.09198.G7F) on U2301 at XBuild batch run config
	12/29	68	Not use Liteon LED(83.00322.070) for package
	12/30	5	Add DUMMY diode EC506 for BUF_CPU_RST# as EMI suggestion
	12/30	42	PC4227 change to 78.33420.5FL as 78.33423.5FL obsoleted
	12/30	49	Change R4904 to short pad
	12/31	86	Add probe point for P2800_VGA_DNX/P2800_VGA_DXP
	01/03	68	Change TPLED1,2 1st to 83.01921.P70 ,2nd to 83.00190.S7A,3rd to 83.00191.H70; R6813 change to 390R from 1K same as DN13 LED part.
	01/03	49	Delete R4908, R4909 for USB_Camera not co-lay
	01/03	4-10	Add 3rd foxconn(62.10055.321) on CPU1 at X-Build batch run config
	01/03	82	Add 3rd T-conn(20.F1932.040) on CRTDB1at X-Build batch run config
	01/03	97	Add 3rd LIDON(34.4CK01.501) on HHD1,HHD4,HGPU1,HGPU2 at X-Build batch run config
	01/04	68	Delete 83.00191.H70 for TPLED1,2 as cost high
	01/04	49,57,75	Add 2nd TAI-TECH(69.10084.071) on TR4901,TR4902,TR5701,TR7501 at X-Build batch run config

<Core Design>



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size  
A3

Document Number  
QUEEN 15

Rev  
A00

Date: Tuesday, January 04, 2011

Sheet 108 of 108